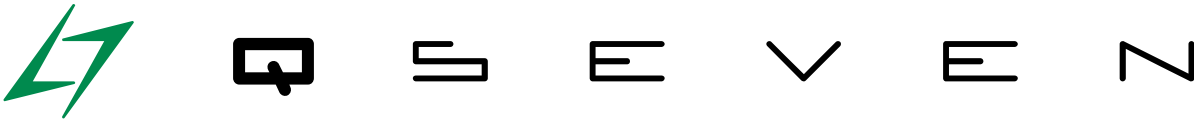
Qseven® Specification

Qseven® pinout, electromechanical description and implementation guidelines



Version 2.0 September 20, 2012

Revision History

Revision	Date (yyyy-mm-dd)	Author	Revision History
1.0	2008-07-01	Qseven® Consortium	Official Release
1.1	2008-08-04	Qseven® Consortium	Corrected overall height dimension in Figure 1-1 Overall Height including Heatspreader of the Qseven® Module. Changed pin assignment in Figure 1-3 Edge Connector Dimensions of the Qseven® Module from Pin 1 to Pin 2.
1.11	2008-11-26	Qseven® Consortium	Corrected the part numbers for the Foxconn connectors and added the part numbers for the Speedtech connectors listed in Table 1-1 MXM Connector. Added mounting hole dimensions for bottom side to Figure 1-2 Mechanical Dimensions of the Qseven® Module. Corrected and added more dimensions to Figure 1-3 Edge Connector Dimensions of the Qseven® Module. Added THRMTRIP# signal description to Table 3-19 Signal Definition Thermal Management. Renamed pin 91 from USB_CL_PRES to USB_HOST_PRES#. Added pin 92 USB_HC_SEL to Table 3-1 Connector Pinout Description and the definition of this signal to Table 3-7 Signal Definition USB. Added pin 204 MFG_NC4 to Table 3-1 Connector Pinout Description. Removed signal pin 56 SDIO_PWRSEL because it is obsolete according to the current SDIO specification and set it to RSVD. Changed the signal description for SDIO_WP I/O column in table 3-8 SDIO Interface Signals from O to I/O. Changed reference to Winbond 83627HG in section 5.1.1 LPC Super I/O Support to Winbond 83627DHG. Added the information about BIOS support for the MAX5362 DAC to section 5.2.7 LCD Control.
1.20	2010-08-12	Qseven® Consortium	Changed component height value for carrier board components located under Qseven® module. Added Figure 1-1 . Added section 1.1.4 Connector and Cooling Plate Keep-Out and Figure 1-6 . Added note and updated connector vendor list in Table 1-1 to include only Qseven® Consortium members. Reduced minimum PCI Express links from 2 to 1, the minimum LPC Bus from 1 to 0 and the minimum HDA/AC'97 interface from 1 to 0 in Table 2-1 . Added ARM/RISC Based Minimum Configuration column to Table 2-1 . Changed note in section 3.2 Input Power Requirements. Changed naming convention in Table 3-1 of pin 91 from USB_HOST_PRES# to USB_CC, pin 92 from USB_HC_SEL to USB_ID in order to be compliant with OTG specification and defined alternative functionality for pins 41, 123, 125, 127, 194, 195, and 196. Also in Table 3-1 changed pin 129 from RSVD to CAN0_TX and pin 130 from RSVD CAN0_RX, pins 199-203 changed from RSVD to SPI interface pins. Added important note to Table 3-2 . Changed name and the signal description in Table 3-7 for USB_HOST_PRES# to USB_CC and BIOS_DISABLE#/BOOT_ALT# and changed the name of USB_HC_SEL to USB_ID. Changed I/O type in Table 3-5 for GBE_LINK#, GBE_LINK100#, GBE_LINK1000# and GBE_ACT# from OD to PP. Changed I/O type for RSTBTN#, BATLOW#, WAKE#, SLP_BTN#, LID_BTN#, and WDTRIG# from OD to CMOS. Added AC'97 support to Table 3-9 . Added CAN Bus Interface Signals section 3.1.13 and Table 3-15 . Added SPI Interface Signals section 3.1.12 and Table 3-14 . Changed description for pins MFG_NC0...4 in Table 3-20 . Updated section 5.2 .

Revision	Date (yyyy-mm-dd)	Author	Revision History
2.0	2012-09-20	Qseven® Consortium	Updated section 1 with the reduced allowable component height on the bottom side of the Qseven module. Updated MXM connector manufacturer Table 1-1. Added Yamaichi footprint proposal (Figure 1-11). Combined DP and HDMI hot plug detection signal on pin 153. Introduced µQseven with 70x40 mm outline. Updated Figure 1-1, Figure 1-2 and Figure 1-6. Added Figure 1-4, Figure 1-7 and Figure 1-11. Changed I2C_CLK to GP0_I2C_CLK. Changed I2C_DAT to GP0_I2C_DAT. Added GPIOs to LPC bus interface. Updated I/O status in Table 3-13 to I/O. Pin 132/134 and 144/146 are set to RSVD (differential pair). Set pin 124 to 1-wire-bus. Set 154 to RSVD. Deleted Express Card and SDVO Interface of Qseven® module from Table 3-1. Deleted MXM connector dimensions figure from specification. Added USB3.0, I2S, UART, eDP, One-Wire-Bus in Table 3-1. Updated SATA Gen1 Signal Budget in Table 4-3. Added Table 4-4 SATA Gen2 Signal Budget. Updated USB2.0 Signal Budget in Table 4-5.
2.0 SGeT	2013-02-23	SGeT e.V.	Added SGeT Copyright page. Updated disclaimers and header/footer layout following SGeT Guidelines. Technical Content unchanged.

Preface

Qseven®Concept

The Qseven® concept is an off-the-shelf, multi vendor, Single-Board-Computer that integrates all the core components of a common PC and is mounted onto an application specific carrier board. Qseven® modules have a standardized form factor of 70mm x 70mm and have specified pinouts based on the high speed MXM system connector that has a standardized pinout regardless of the vendor. The Qseven® module provides the functional requirements for an embedded application. These functions include, but are not limited to, graphics, sound, mass storage, network and multiple USB ports. A single ruggedized MXM connector provides the carrier board interface to carry all the I/O signals to and from the Qseven® module. This MXM connector is a well known and proven high speed signal interface connector that is commonly used for high speed PCI Express graphics cards in notebooks.

Carrier board designers can utilize as little or as many of the I/O interfaces as deemed necessary. The carrier board can therefore provide all the interface connectors required to attach the system to the application specific peripherals. This versatility allows the designer to create a dense and optimized package, which results in a more reliable product while simplifying system integration. Most importantly, Qseven® applications are scalable, which means once a product has been created there is the ability to diversify the product range through the use of different performance class Qseven® modules. Simply unplug one module and replace it with another, no redesign is necessary.

Qseven® offers the newest I/O technologies on this minimum size form factor. This includes serial high speed buses such as:

- PCI Express™
- USB 3.0
- Serial ATA ®
- Secure Digital I/O interface
- DisplayPort™, TMDS
- USB 2.0
- High Definition Digital Audio (HDA) Integrated Interchip Sound (I2S)
- LPC interface
- Gigabit Ethernet
- LVDS Display Interface

Plus additional control and power management signals.

Disclaimer

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This Qseven®electromechanical specification is intended for technically qualified personnel. It is not intended for general audiences.

Symbols

The following symbols may be used in this specification:

Warning

Warnings indicate conditions that, if not observed, can cause personal injury.

Caution

Cautions warn the user about how to prevent damage to hardware or loss of data.

Note

Notes call attention to important information that should be observed.

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All Qseven®designs shall be created from lead-free components in order to be RoHS compliant.

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The Qseven® logo is freely available for members of SGeT e.V.. The logo can only be applied to products that are fully compliant to the specification of the Qseven® standard.

SGeT e.V. reserves the right to take legal action against any party that fails to comply with the rules stated above for Qseven® logo usage.

High resolution formats are available at the members area www.qseven-standard.org .

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Terminology

Term	Description
ARM/RISC	The ARM is a 32-bit reduced instruction set computer (RISC) instruction set architecture (ISA) developed by ARM Holdings.
X86	The term x86 refers to a family of instruction set architectures based on the Intel 8086.
PCI Express (PCIe)	Peripheral Component Interface Express. Next-generation high speed serialized I/O bus
PCI Express Lane	One PCI Express Lane is a set of 4 signals that contains two differential lines for Transmitter and two differential lines for Receiver. Clocking information is embedded into the data stream.
x1, x2, x4	x1 refers to one PCI Express Lane of basic bandwidth; x2 to a collection of two PCI Express Lanes; etc.. Also referred to as x1, x2, x4 link.
DDC	Display Data Channel is an I²C bus interface between a display and a graphics adapter.
DVI	Digital Visual Interface is a video interface standard developed by the Digital Display Working Group (DDWG).
GBE	Gigabit Ethernet
USB	Universal Serial Bus
SATA	Serial AT Attachment: serial interface standard for hard disks.
HDA	High Definition Audio
I2S	Integrated Interchip Sound (I2S) is an electrical serial bus interface standard used for connecting digital audio devices together.
HDMI	High Definition Multimedia Interface. HDMI supports standard, enhanced, or high-definition video, plus multi-channel digital audio on a single cable.
TMDS	Transition Minimized Differential Signaling. TMDS is a signaling interface defined by Silicon Image that is used for DVI and HDMI.
DP eDP	(embedded) DisplayPort (DP/eDP) is a digital display interface developed by the Video Electronics Standards Association (VESA).
LPC	Low Pin-Count Interface: a low speed interface used for peripheral circuits such as Super I/O controllers, which typically combine legacy-device support into a single IC.
CAN	Controller Area Network
SPI	Serial Peripheral Interface
SDIO	Secure Digital Input Output
SMB	System Management Bus
LVDS	Low-Voltage Differential Signaling
ACPI	Advanced Control Programmable Interface
RoHS	Restriction on Hazardous Substances: The Directive on the Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment 2002/95/EC.
N.C.	Not connected
N.A.	Not available
T.B.D.	To be determined

Contents

Tables

Figures

1 Qseven® Mechanical Characteristics

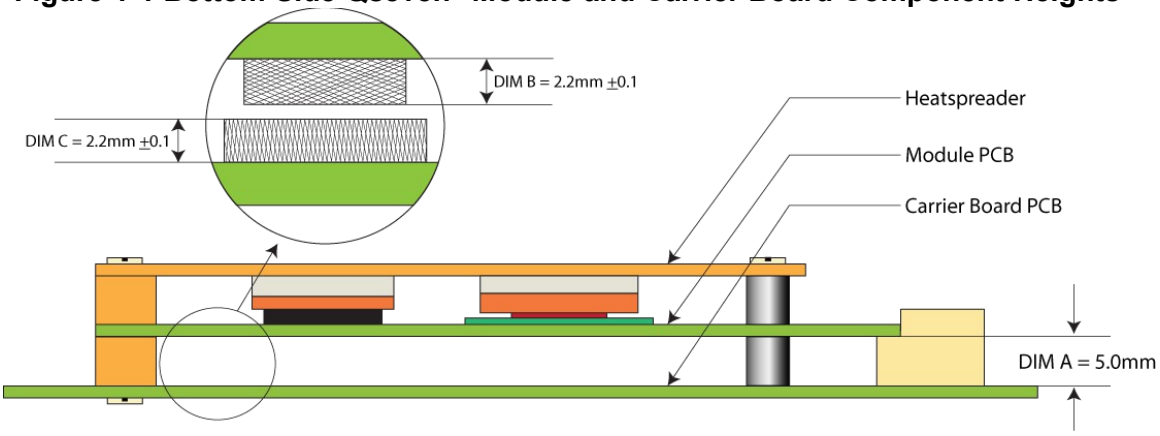
The Qseven® module, including the heatspreader plate, PCB thickness and bottom components, is up to approximately 12mm thick.

Edge-fingers on the module are referenced to the PCB slot center with an overall PCB thickness of 1.2mm ±0.1 measured across the fingers including the plating and/or metalization on both sides. Bevel is optional, but edge shall be free of burrs and shall not have sharp edges.

The components located on the top side of the module are up to 5.5mm high. Components mounted on the backside of the Qseven® module (in the space between the bottom surface of the module PCB and the top surface of the carrier board PCB) shall have a height of 2.2mm ±0.1 (dimension 'B' in Figure 1-1). When using a MXM connector with a resulting height between carrier board and Qseven® module of 2.7mm, carrier board component placement below the Qseven® module is prohibited.

Carrier board component placement below the Qseven® module is only permitted when using a MXM connector with a resulting height between carrier board and Qseven® module of 5.0mm (dimension 'A' in Figure 1-1) and no carrier board component shall exceed a height of 2.2mm ±0.1 (dimension 'C' in Figure 1-1). Using carrier board topside components up to 2.2mm allows a gap of 0.3mm between carrier board topside components and the Qseven® module bottom side components. This may not be sufficient in some situations. In carrier board applications in which vibration or board flex is a concern, then the carrier board component height should be restricted to a value less than 2.2mm that yields a clearance that is sufficient for the application. Refer to Table 1-1 regarding MXM connector specifications.

Figure 1-1 Bottom Side Qseven® Module and Carrier Board Component Heights

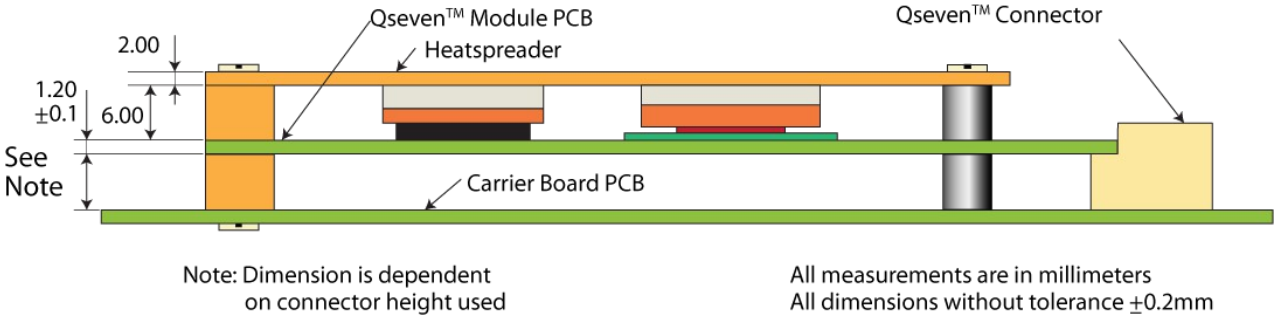


The heatspreader offered for Qseven® modules acts as a thermal coupling device and is not a heat sink. Heat dissipation devices such as a heat sink with fan or heat pipe may need to be connected to the heatspreader. The dissipation of heat will fluctuate between different CPU boards. Refer to the Qseven® module's user's guide for heatspreader dimensions and specifications.

The standoffs for the heatspreader and carrier board must not exceed 5.6mm overall external diameter. This ensures that the standoff contact area does not exceed the defined mounting hole footprint on the Qseven® module. The screw that is to be used for mounting must be a metric thread M2.5 DIN7985 / ISO7045.

Qseven® modules are defined to feature ultra low power CPU and chipset solutions with an ultra low “Thermal Design Power” (TDP). Furthermore, the modules power consumption should not exceed 12W.

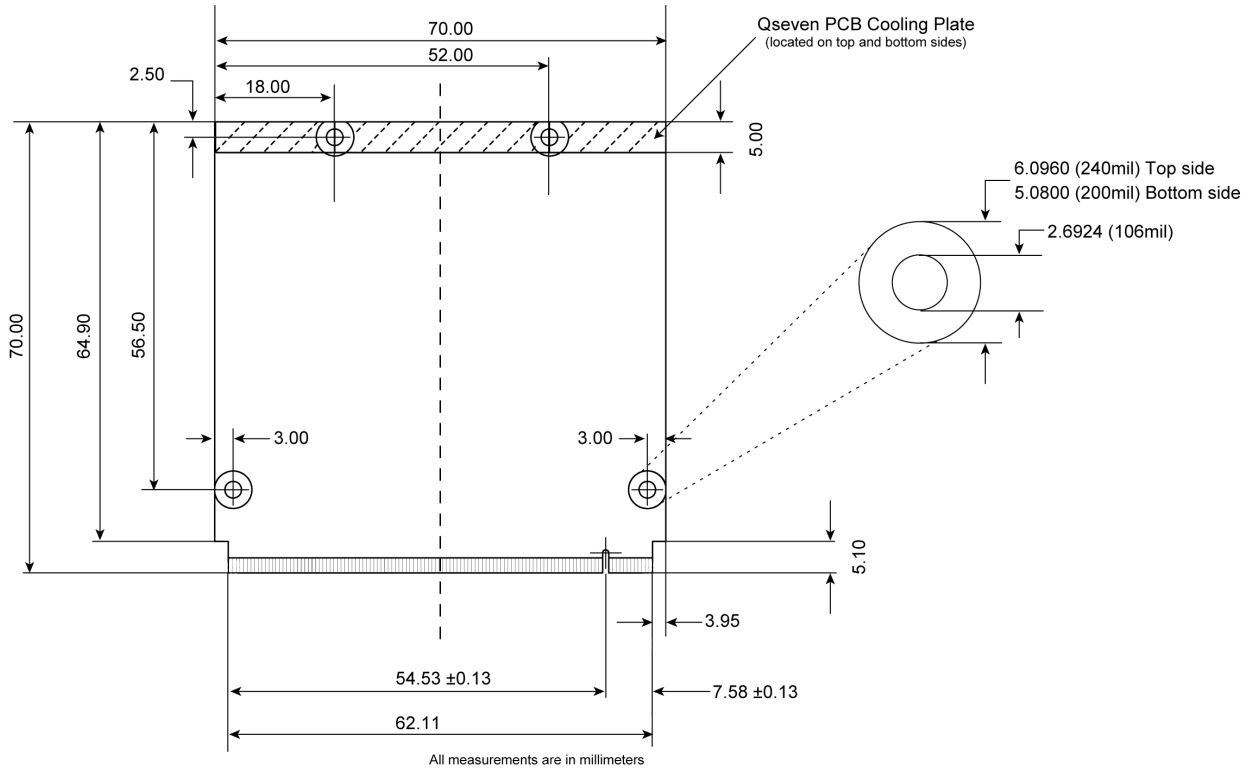
Figure 1-2 Overall Height including Heatspreader of the Qseven® Module



1.1 Mechanical Dimensions

1.1.1 Qseven® Module Outline

Figure 1-3 Mechanical Dimensions of the Qseven® Module

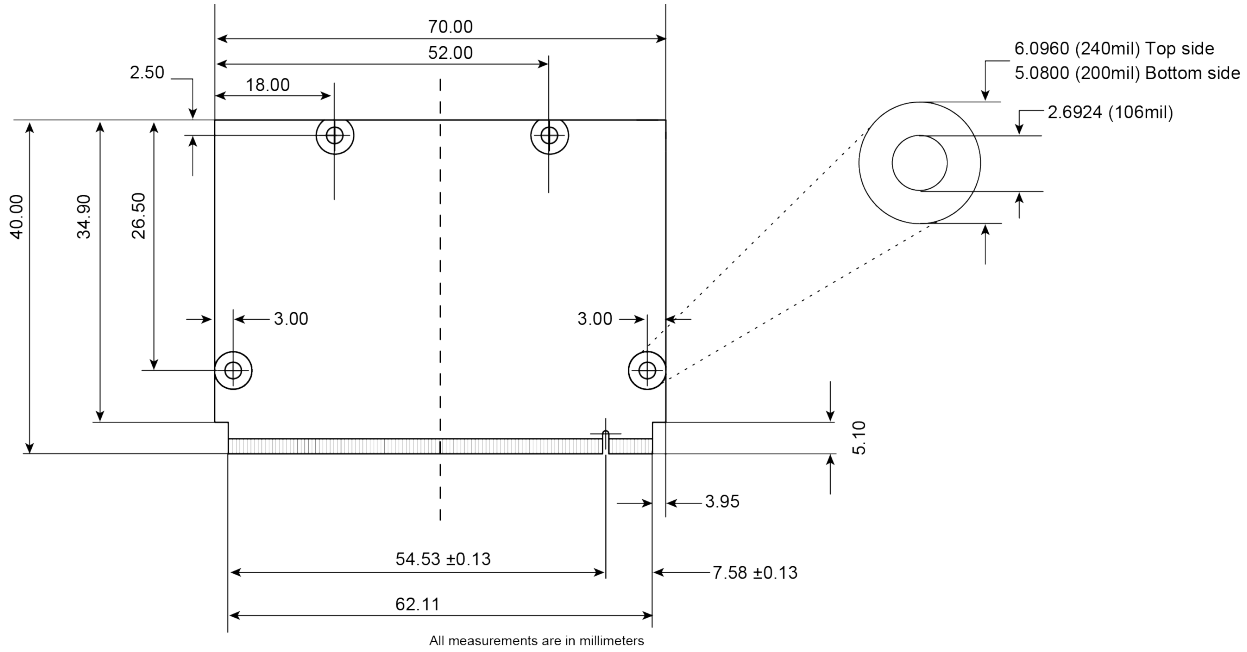


Qseven Module Top Side

The Qseven® PCB cooling plate shown in Figure 1-3 is to be used as a cooling interface between the Qseven® module and the application specific cooling solution.

1.1.2 µQseven Module Outline

Figure 1-4: Mechanical Dimension of the µQseven Module



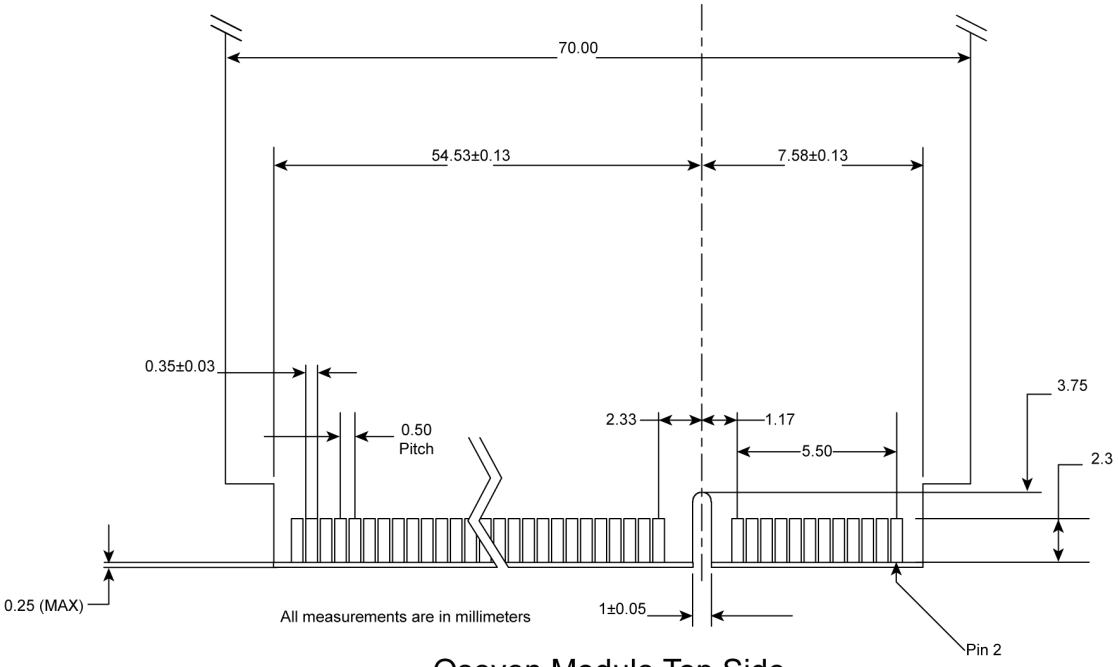
Qseven Module Top Side

Note

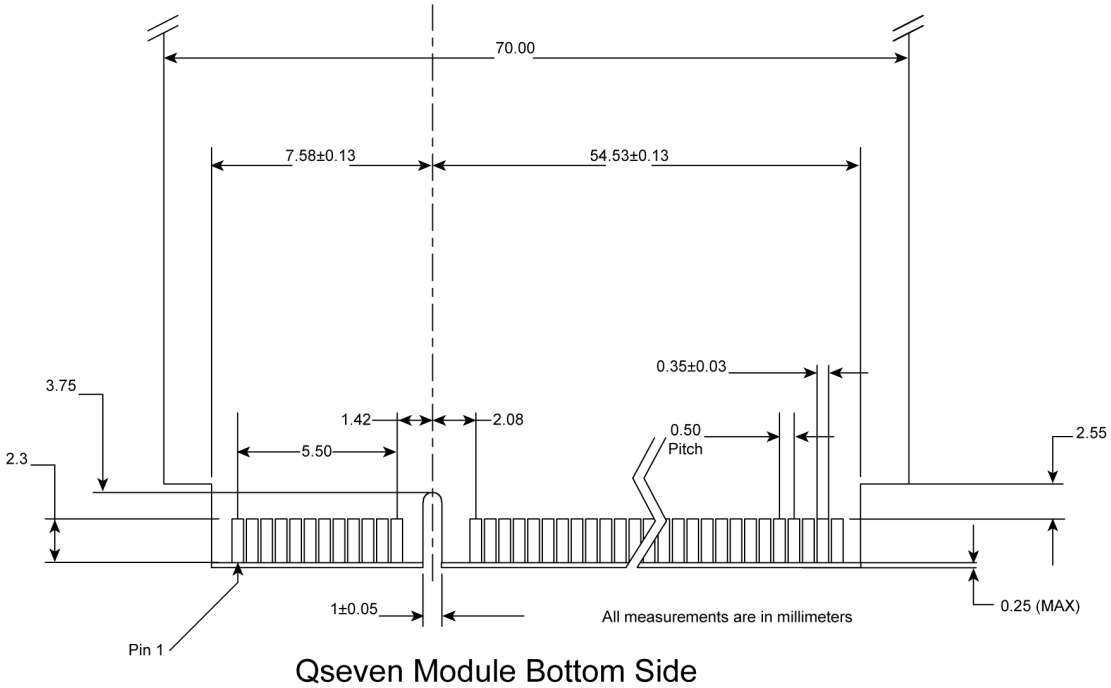
If one carrier board design is used for both µQseven and Qseven®, the standoffs of the smaller µQseven module will collide with the Qseven® module . To support both outlines, these standoffs of the µQseven module should be removed when full sized Qseven® modules are used.

1.1.3 Edge Connector Dimensions of the PCB

Figure 1-5 Edge Connector Dimensions of the Qseven® Module



Qseven Module Top Side



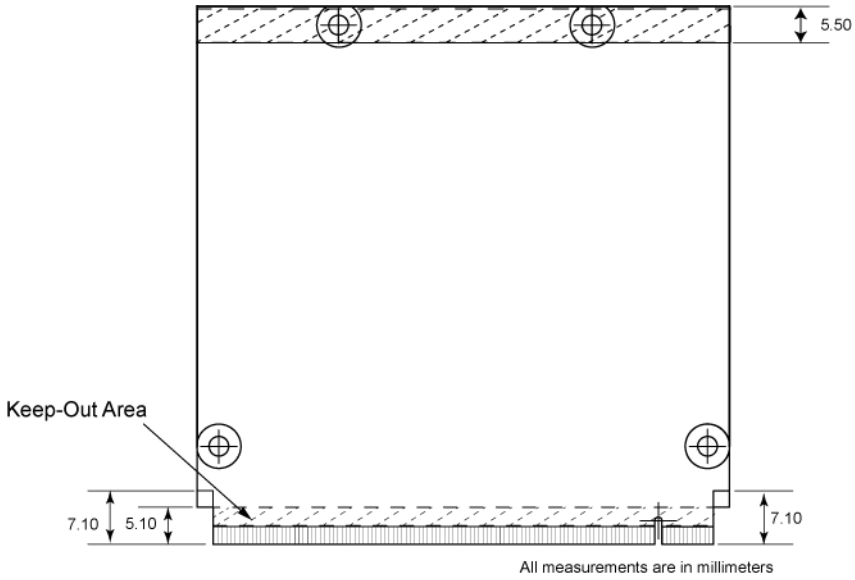
Qseven Module Bottom Side

Note

It is important to note that the edge fingers found on the top and bottom side are not mirrored and therefore have a slight offset from topside to bottom side.

1.1.4 Connector and Cooling Plate Keep-Out

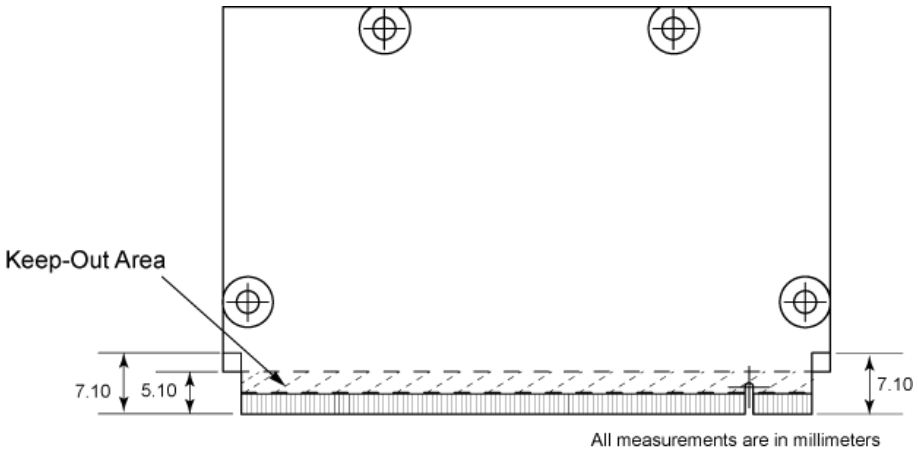
Figure 1-6 Qseven® Connector and Cooling Plate Keep-Out Area



Qseven Connector and
Cooling Plate Keep Out Area
(Top and Bottom side)

It is not permitted to place components within the keep-out area defined above in order to avoid any mechanical collisions between components.

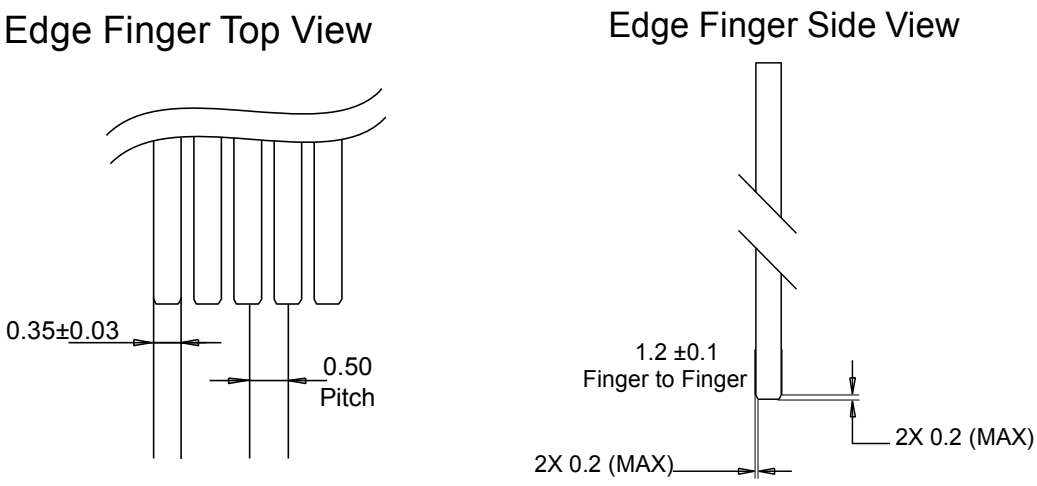
Figure 1-7: µQseven Keep-Out Area



Qseven Connector and
Cooling Plate Keep Out Area
(Top and Bottom side)

1.1.5 Single Edge Finger Dimensions

Figure 1-8 Edge Finger Dimensions of the Qseven® Module



Note

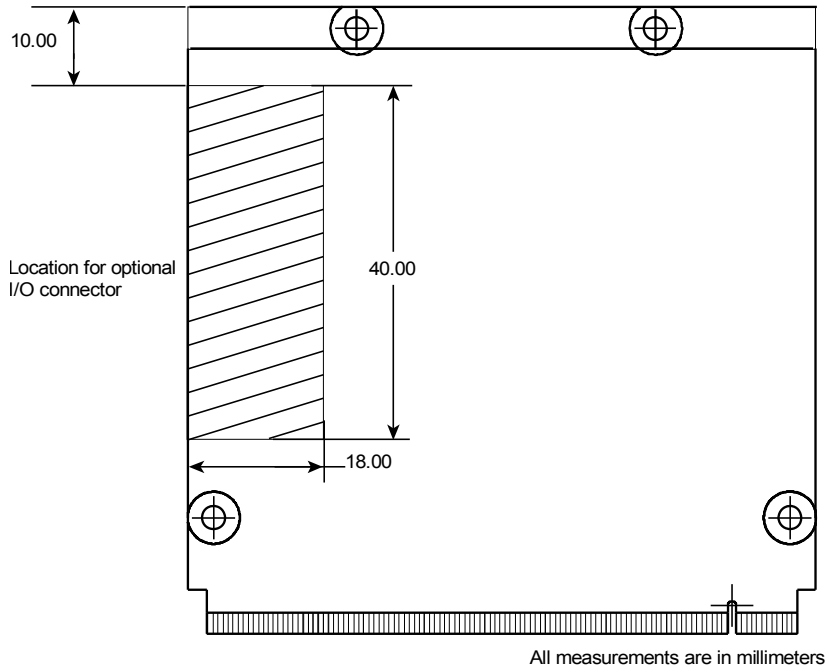
Edge fingers are the same for both modules outlines.

1.1.6 Location for Optional I/O Connector

If an optional I/O connector, such as a Video Capture Port (VCP), is to be used it shall be placed in the I/O connector location area as defined in Figure 1-9.

This area is not a keep-out area and can be used for component placement if no additional I/O connector is required.

Figure 1-9 Optional I/O Connector Area



Qseven Module Top Side

Note

No location for an I/O connector is defined for µQseven Module.

1.2 MXM Connector

The Qseven® module utilizes a 230-pin card-edge connector that is also used for PCI Express capable notebook graphics cards following the MXM specification. Therefore, this connector type is also known as a MXM connector.

The MXM edge connector is the result of an extensive collaborative design effort with the industry's leading notebook manufacturers. This collaboration has produced a robust, low-cost edge connector that is capable of handling high-speed serialized signals.

The MXM connector accommodates various connector heights for different carrier board applications needs. This specification suggests two connector heights, 7.8mm and 7.5mm.

Table 1-1 MXM Connector

Manufacturer	Part Number	Specification	Resulting height between carrier board and Qseven® module	Overall height of the MXM Connector
Aces	88882-2Dxx	88882-2Dxx	5.0mm	7.5mm
Yamaichi	BEC05230S9xFREDC	BEC05230S9xFREDC	5.0 mm	7.8 mm
Foxconn	AS0B32x-S78N-xH	AS0B32x-S78N-xH	5.0 mm	7.8 mm

Note

The connectors mentioned in Table 1-1 are only a partial list of what is offered by the manufacturers. For more information about additional variants contact the manufacturer.

1.2.1 Environmental Characteristics

Table 1-2 Environmental Characteristics for MXM Connectors

Parameter	Specification
Durability	EIA-364-9 30 cycles
Mating and unmating force	EIA-364-13C LIF/angled insertion styled cards: Maximum insertion force: 1.3 kg Maximum extraction force: 1.6 kg Slide-in/side insertion styled cards Maximum insertion force: 6.0 kg Maximum extraction force: 4.6 kg *Note: numbers tabulated using a velocity of 25 mm/min*
Vibration	EIA-364-28D – Test condition VII condition D With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type III PCB
Shock	EIA-364-27B – Test condition A With a 40 x 40 mm block of 100 grams fastened and centered at the GPU center of a Type III PCB

1.2.2 Electrical Characteristics

Table 1-3 Electrical Characteristics for MXM Connectors

Parameter	Specification
Low Level Contact Resistance	EIA-364-23B – Specify which option used. Do not use option 4. Requirement: 40 mΩ maximum for initial measurements 50 mΩ maximum or Delta R = 20 mΩ maximum, whichever is less, for measurements after other tests
Insulation Resistance	EIA-364-21C Requirements: Initial testing 250 MΩ. 50 MΩ after other test procedures
Dielectric Withstanding Voltage	EIA-364-20B – Method B on one pair of upper adjacent contacts and on one pair of lower adjacent contacts. Connector is unmated and unmounted. Barometric pressure at sea level. Apply 0.25 kV AC, (50 Hz) for 1 minute.
Current Rating	Current requirement: Pins rated for 0.5 Amp continuous The temperature rise above ambient shall not exceed 30 °C, where ambient condition is 25 °C still air.
Voltage Rating	50VDC per contact
Impedance	EIA-364-108 Impedance Requirements: 100 ± 20 Ω differential, 50 ± 10 Ω single ended.
Insertion Loss	EIA-364-101 Insertion Loss Requirements: 1 dB max up to 1.25 GHz; ≤ [1.6* (F-1.25)+1] dB for 1.25 GHz < F ≤ 3.75 GHz (for example, ≤ 5 dB at F = 3.75 GHz) where F is frequency in GHz.
Return Loss	EIA-364-108 Return Loss Requirements: ≤ -12 dB up to 1.3 GHz ≤ -7dB up to 2 GHz ≤ -4 dB up to 3.75 GHz
Near End Crosstalk	EIA-364-90 Crosstalk(NEXT) Requirements: -32 dB max up to 1.25 GHz ≤ -[32 – 2.4* (F – 1.25)] dB for 1.25 GHz < F ≤ 3.75 GHz (for example, ≤ -26 dB at F = 3.75 GHz) where F is frequency in GHz.

1.2.3 MXM Connector Dimensions

Note

Refer to the used MXM connector's manufacturer's datasheet for information about the dimensions of the MXM connector.

1.2.4 MXM Connector Footprint

Figure 1-10 Carrier Board PCB Footprint for Foxconn MXM Connector

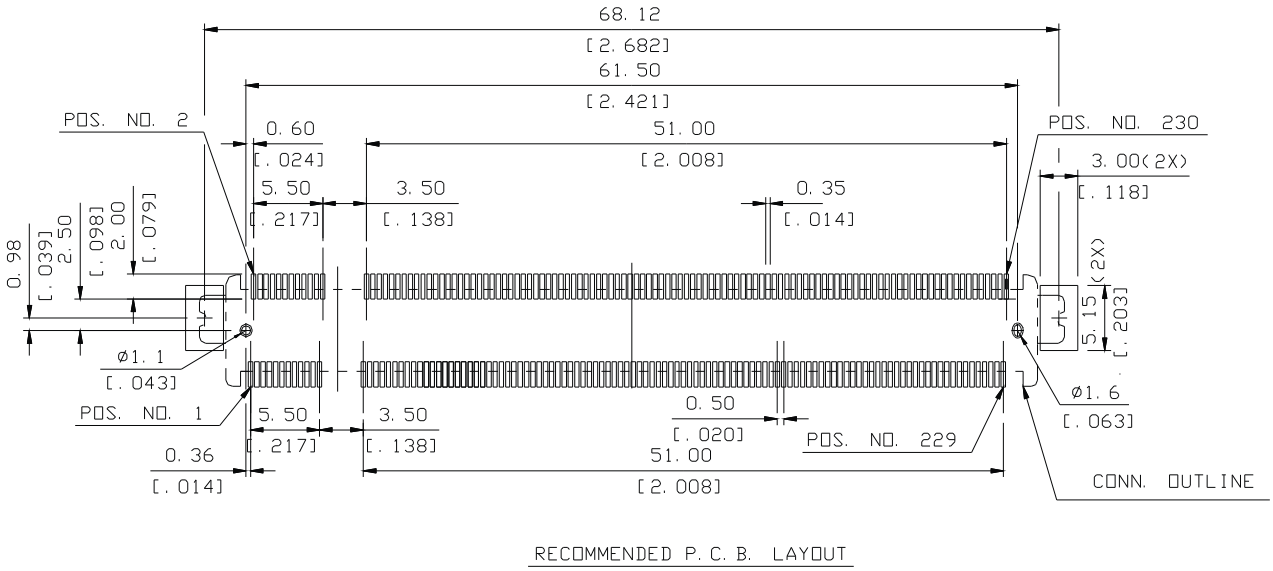
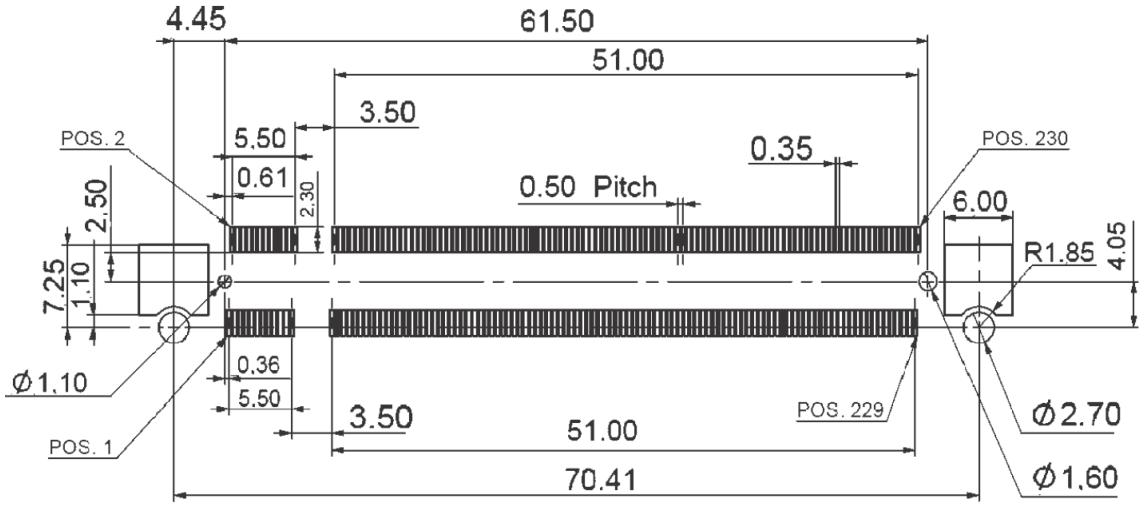


Figure 1-11 Carrier Board PCB Footprint for Yamaichi MXM Connector



Note

The connectors mentioned in Table 1-1 are only a partial list of what is offered by the manufacturers. For more information about additional variants contact the manufacturer. Refer to the datasheet of the vendor for more details about the footprint. The footprints can slightly vary between different vendors.

2 Qseven® Feature Overview

The Qseven® mandatory and optional features. Table 2-1 shows the minimum and maximum required configuration of the feature set.

Table 2-1Qseven® Supported Features

System I/O Interface	ARM/RISC Based Minimum Configuration	X86 Based Minimum Configuration	Maximum Configuration
PCI Express lanes	0	1 (x1 link)	4
Serial ATA channels	0	0	2
USB 2.0 ports	3	4	8
USB 3.0 ports	0	0	2
LVDS channels embedded DisplayPort	0 0	0 0	Dual Channel 24bits 2
DisplayPort, TMDS	0	0	1
High Definition Audio / AC'97 / I2S	0	0	1
Ethernet 10/100 Mbit/Gigabit	0	0	1 (Gigabit Ethernet)
UART	0	0	1
Low Pin Count bus	0	0	1
Secure Digital I/O 8-bit for SD/MMC cards	0	0	1
System Management Bus	0	1	1
I²C Bus	1	1	1
SPI Bus	0	0	1
CAN Bus	0	0	1
Watchdog Trigger	1	1	1
Power Button	1	1	1
Power Good	1	1	1
Reset Button	1	1	1
LID Button	0	0	1
Sleep Button	0	0	1
Suspend To RAM (S3 mode)	0	0	1
Wake	0	0	1
Battery low alarm	0	0	1
Thermal control	0	0	1
FAN control	0	0	1

3 Connector Pin Assignments

There are 115 edge fingers on the top and bottom side of the Qseven® module that mate with the MXM connector. Table 3-1 lists the pin assignments for all 230 edge fingers.

Table 3-1 Connector Pinout Description

Pin	Signal	Pin	Signal
1	GND	2	GND
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	SUS_STAT#	20	PWRBTN#
21	SLP_BTN#	22	LID_BTN#
23	GND	24	GND
	KEY		KEY
25	GND	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	GND
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	GND	40	GND
41	BIOS_DISABLE# / BOOT_ALT#	42	SDIO_CLK#
43	SDIO_CD#	44	SDIO_LED
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DAT1
49	SDIO_DAT0	50	SDIO_DAT3
51	SDIO_DAT2	52	SDIO_DAT5
53	SDIO_DAT4	54	SDIO_DAT7
55	SDIO_DAT6	56	RSVD
57	GND	58	GND
59	HDA_SYNC / I2S_WS	60	SMB_CLK / GP1_I2C_CLK
61	HDA_RST# / I2S_RST#	62	SMB_DAT / GP1_I2C_DAT
63	HDA_BITCLK / I2S_CLK	64	SMB_ALERT#
65	HDA_SDI / I2S_SDI	66	GP0_I2C_CLK
67	HDA_SDO / I2S_SDO	68	GP0_I2C_DAT

Pin	Signal	Pin	Signal
69	THRM#	70	WDTRIG#
71	THRMTRIP#	72	WDOUT
73	GND	74	GND
75	USB_P7- / USB_SSTX0-	76	USB_P6- / USB_SSRX0-
77	USB_P7+ / USB_SSTX0+	78	USB_P6+ / USB_SSRX0+
79	USB_6_7_OC#	80	USB_4_5_OC#
81	USB_P5- / USB_SSTX1-	82	USB_P4- / USB_SSRX1-
83	USB_P5+ / USB_SSTX1+	84	USB_P4+ / USB_SSRX1+
85	USB_2_3_OC#	86	USB_0_1_OC#
87	USB_P3-	88	USB_P2-
89	USB_P3+	90	USB_P2+
91	USB_CC	92	USB_ID
93	USB_P1-	94	USB_P0-
95	USB_P1+	96	USB_P0+
97	GND	98	GND
99	eDP0_TX0+ / LVDS_A0+	100	eDP1_TX0+ / LVDS_B0+
101	eDP0_TX0- / LVDS_A0-	102	eDP1_TX0- / LVDS_B0-
103	eDP0_TX1+ / LVDS_A1+	104	eDP1_TX1+ / LVDS_B1+
105	eDP0_TX1- / LVDS_A1-	106	eDP1_TX1- / LVDS_B1-
107	eDP0_TX2+ / LVDS_A2+	108	eDP1_TX2+ / LVDS_B2+
109	eDP0_TX2- / LVDS_A2-	110	eDP1_TX2- / LVDS_B2-
111	LVDS_PPEN	112	LVDS_BLEN
113	eDP0_TX3+ / LVDS_A3+	114	eDP1_TX3+ / LVDS_B3+
115	eDP0_TX3- / LVDS_A3-	116	eDP1_TX3- / LVDS_B3-
117	GND	118	GND
119	eDP0_AUX+ / LVDS_A_CLK+	120	eDP1_AUX+ / LVDS_B_CLK+
121	eDP0_AUX- / LVDS_A_CLK-	122	eDP1_AUX- / LVDS_B_CLK-
123	LVDS_BLT_CTRL /GP_PWM_OUT0	124	GP_1-Wire_Bus
125	GP2_I2C_DAT / LVDS_DID_DAT	126	eDP0_HPD# / LVDS_BLC_DAT
127	GP2_I2C_CLK / LVDS_DID_CLK	128	eDP1_HPD# / LVDS_BLC_CLK
129	CAN0_TX	130	CAN0_RX
131	DP_LANE3+ / TMDS_CLK+	132	RSVD (Differential Pair)
133	DP_LANE3- / TMDS_CLK-	134	RSVD (Differential Pair)
135	GND	136	GND
137	DP_LANE1+ / TMDS_LANE1+	138	DP_AUX+
139	DP_LANE1- / TMDS_LANE1-	140	DP_AUX-
141	GND	142	GND
143	DP_LANE2+ / TMDS_LANE0+	144	RSVD (Differential Pair)
145	DP_LANE2- / TMDS_LANE0-	146	RSVD (Differential Pair)
147	GND	148	GND

Pin	Signal	Pin	Signal
149	DP_LANE0+ / TMDS_LANE2+	150	HDMI_CTRL_DAT
151	DP_LANE0- / TMDS_LANE2-	152	HDMI_CTRL_CLK
153	DP_HDMI_HPD#	154	RSVD
155	PCIE_CLK_REF+	156	PCIE_WAKE#
157	PCIE_CLK_REF-	158	PCIE_RST#
159	GND	160	GND
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_TX-	164	PCIE3_RX-
165	GND	166	GND
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	UART0_TX	172	UART0_RTS#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	UART0_RX	178	UART0_CTS#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	GND	184	GND
185	LPC_AD0 / GPIO0	186	LPC_AD1 / GPIO1
187	LPC_AD2 / GPIO2	188	LPC_AD3 / GPIO3
189	LPC_CLK / GPIO4	190	LPC_FRAME# / GPIO5
191	SERIRQ / GPIO6	192	LPC_LDRQ# / GPIO7
193	VCC_RTC	194	SPKR / GP_PWM_OUT2
195	FAN_TACHOIN / GP_TIMER_IN	196	FAN_PWMOUT / GP_PWM_OUT1
197	GND	198	GND
199	SPI_MOSI	200	SPI_CS0#
201	SPI_MISO	202	SPI_CS1#
203	SPI_SCK	204	MFG_NC4
205	VCC_5V_SB	206	VCC_5V_SB
207	MFG_NC0	208	MFG_NC2
209	MFG_NC1	210	MFG_NC3
211	VCC	212	VCC
213	VCC	214	VCC
215	VCC	216	VCC
217	VCC	218	VCC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

3.1 Signal Descriptions

The “#” symbol at the end of the signal name indicates that the active, or asserted state, occurs when the signal is at a low voltage level. When “#” is not present, the signal is asserted when at a high voltage level. Differential pairs are indicated by trailing '+' and '-' signs for the positive or negative signal.

The following terminology is used to describe the signals types in the I/O columns for the tables located below.

Table 3-2 Signal Terminology

Term	Description
I	Input Pin
O	Output Pin
OC	Open Collector
OD	Open Drain
PP	Push Pull
I/O	Bi-directional Input/Output Pin
I_{OL}	Output low current The I_{OL} is the maximum output low current the module must be able to drive to an external circuitry.
I_{IL}	Input low current The I_{IL} is the maximum input low current that must be provided to the Qseven® module via external circuitry in order to guarantee a proper logic low level of the signal.
P	Power Input
NC	Not Connected
PCIE	PCI Express differential pair signals. In compliance with the PCI Express Base Specification 1.1.
GB_LAN	Gigabit Ethernet Media Dependent Interface differential pair signals. In compliance with IEEE 802.3ab 1000Base-T Gigabit Ethernet Specification.
USB	Universal Serial Bus differential pair signals In compliance with the Universal Serial Bus Specification 2.0
SATA	Serial Advanced Technology Attachment differential pair signals. In compliance with the Serial ATA High Speed Serialized AT Attachment Specification 1.0a.
LVDS	Low-Voltage Differential Signaling differential pair signals. In compliance with the LVDS Owner's Manual 4.0.
TMDS	Transition Minimized Differential Signaling differential pair signals. In compliance with the Digital Visual Interface (DVI) Specification 1.0.
CMOS	Logic input or output.

Important information

All required pull-ups or pull-down resistors shall be implemented on the Qseven® module. These onboard terminations shall be designed according to the EDG (Engineering Design Guide) of the used CPU platform.

3.1.1 PCI Express Interface Signals

Table 3-3 Signal Definition PCI Express

Signal	Description	I/O Type	I_{OL}/I_{IIL}	I/O
PCIE0_RX+ PCIE0_RX-	PCI Express channel 0, Receive Input differential pair.	PCIE		I
PCIE0_TX+ PCIE0_TX-	PCI Express channel 0, Transmit Output differential pair.	PCIE		O
PCIE1_RX+ PCIE1_RX-	PCI Express channel 1, Receive Input differential pair.	PCIE		I
PCIE1_TX+ PCIE1_TX-	PCI Express channel 1, Transmit Output differential pair.	PCIE		O
PCIE2_RX+ PCIE2_RX-	PCI Express channel 2, Receive Input differential pair.	PCIE		I
PCIE2_TX+ PCIE2_TX-	PCI Express channel 2, Transmit Output differential pair.	PCIE		O
PCIE3_RX+ PCIE3_RX-	PCI Express channel 3, Receive Input differential pair.	PCIE		I
PCIE3_TX+ PCIE3_TX-	PCI Express channel 3, Transmit Output differential pair.	PCIE		O
PCIE_CLK_REF+ PCIE_CLK_REF-	PCI Express Reference Clock for Lanes 0 to 3.	PCIE		O
PCIE_WAKE#	PCI Express Wake Event: Sideband wake signal asserted by components requesting wakeup.	CMOS 3.3V Suspend	≥ 5 mA	I
PCIE_RST#	Reset Signal for external devices.	CMOS 3.3V	max 1 mA	O

Note

There are a total of 4 PCI Express TX and RX differential pairs supported on the Qseven® module. Depending on the features supported by the Qseven® module and the core logic chipset used, these lines may be used to form x1 or x4 PCI Express links. The documentation for the Qseven® module shall clearly identify, which PCI Express link configuration or configurations (in the case that these can be programmed in the core logic chipset) are supported.

3.1.2 UART Interface Signals

Table 3-4 Signal Definition of UART

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
UART0_TX	Serial Data Transmitter	CMOS 3.3V	max 1 mA	O
UART0_RX	Serial Data Reciever	CMOS 3.3V	≥ 5 mA	I
UART0_CTS#	Handshake signal, ready to send data	CMOS 3.3V	≥ 5 mA	I
UART0_RTS#	Handshake signal, ready to receive data	CMOS 3.3V	max. 1 mA	O

3.1.3 Gigabit Ethernet Signals

Table 3-5 Signal Definition Ethernet

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
GBE_MDI0+ GBE_MDI0-	Media Dependent Interface (MDI) differential pair 0. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI1+ GBE_MDI1-	Media Dependent Interface (MDI) differential pair 1. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is used for all modes.	GB_LAN		I/O
GBE_MDI2+ GBE_MDI2-	Media Dependent Interface (MDI) differential pair 2. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_MDI3+ GBE_MDI3-	Media Dependent Interface (MDI) differential pair 3. The MDI can operate in 1000, 100, and 10Mbit/sec modes. This signal pair is only used for 1000Mbit/sec Gigabit Ethernet mode.	GB_LAN		I/O
GBE_CTREF	Reference voltage for carrier board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the module's PHY and may be as low as 0V and as high as 3.3V. The reference voltage output shouldbe current limited on the module. In a case in which the reference is shorted to ground, the current must be limited to 250mA or less.	REF		
GBE_LINK#	Ethernet controller 0 link indicator, active low.	CMOS 3.3V PP	max 10 mA	O
GBE_LINK100#	Ethernet controller 0 100Mbit/sec link indicator, active low.	CMOS 3.3V PP	max 10 mA	O
GBE_LINK1000#	Ethernet controller 0 1000Mbit/sec link indicator, active low.	CMOS 3.3V PP	max 10 mA	O
GBE_ACT#	Ethernet controller 0 activity indicator, active low.	CMOS 3.3V PP	max 10 mA	O

3.1.4 Serial ATA Interface Signals

Table 3-6 Signal Definition SATA

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
SATA0_RX+ SATA0_RX-	Serial ATA channel 0, Receive Input differential pair.	SATA		I
SATA0_TX+ SATA0_TX-	Serial ATA channel 0, Transmit Output differential pair.	SATA		O
SATA1_RX+ SATA1_RX-	Serial ATA channel 1, Receive Input differential pair.	SATA		I
SATA1_TX+ SATA1_TX-	Serial ATA channel 1, Transmit Output differential pair.	SATA		O
SATA_ACT#	Serial ATA Led. Open collector output pin driven during SATA command activity.	OC 3.3V	max. 10mA	O

3.1.5 USB Interface Signals

Table 3-7 Signal Definition USB

Signal	Description	I/O Type	I_{OL} /I_{IL}	I/O
USB_P0+ USB_P0-	Universal Serial Bus Port 0 differential pair.	USB		I/O
USB_P1+ USB_P1-	Universal Serial Bus Port 1 differential pair. This port may be optionally used as USB client port.	USB		I/O
USB_P2+ USB_P2-	Universal Serial Bus Port 2 differential pair.	USB		I/O
USB_P3+ USB_P3-	Universal Serial Bus Port 3 differential pair.	USB		I/O
USB_P4+ USB_P4- USB_SSRX1+ USB_SSRX1-	Universal Serial Bus Port 4 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path.	USB		I/O I
USB_P5+ USB_P5- USB_SSTX1+ USB_SSTX1-	Universal Serial Bus Port 5 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path.	USB		I/O O
USB_P6+ USB_P6- USB_SSRX0+ USB_SSRX0-	Universal Serial Bus Port 6 differential pair. Multiplexed with receive signal differential pairs for the Superspeed USB data path.	USB		I/O I
USB_P7+ USB_P7- USB_SSTX0+ USB_SSTX0-	Universal Serial Bus Port 7 differential pair. Multiplexed with transmit signal differential pairs for the Superspeed USB data path.	USB		I/O O
USB_0_1_OC#	Over current detect input 1. This pin is used to monitor the USB power over current of the USB Ports 0 and 1.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_2_3_OC#	Over current detect input 2. This pin is used to monitor the USB power over current of the USB Ports 2 and 3.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_4_5_OC#	Over current detect input 3. This pin is used to monitor the USB power over current of the USB Ports 4 and 5.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_6_7_OC#	Over current detect input 4. This pin is used to monitor the USB power over current of the USB Ports 6 and 7.	CMOS 3.3V Suspend	≥ 5 mA	I
USB_ID	USB ID pin. Configures the mode of the USB Port 1. If the signal is detected as being 'high active' the BIOS will automatically configure USB Port 1 as USB Client and enable USB Client support. This signal should be driven as OC signal by external circuitry.	CMOS 3.3V Suspend		I
USB_CC	USB Client Connect pin. If USB Port 1 is configured for client mode then an externally connected USB host should set this signal to high-active in order to properly make the connection with the module's internal USB client controller. If the external USB host is disconnected, this signal should be set to low-active in order to inform the USB client controller that the external host has been disconnected. A level shifter/protection circuitry should be implemented on the carrier board for this signal.	CMOS 3.3V Suspend		I

3.1.6 SDIO Interface Signals

SDIO stands for Secure Digital Input Output. Devices that support SDIO can use small devices such as SD-Card or MMC-Card flash memories.

Table 3-8 Signal Definition SDIO

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
SDIO_CD#	SDIO Card Detect. This signal indicates when a SDIO/MMC card is present.	CMOS 3.3V		I/O
SDIO_CLK	SDIO Clock. With each cycle of this signal a one-bit transfer on the command and each data line occurs. This signal has maximum frequency of 48 MHz.	CMOS 3.3V		O
SDIO_CMD	SDIO Command/Response. This signal is used for card initialization and for command transfers. During initialization mode this signal is open drain. During command transfer this signal is in push-pull mode.	CMOS 3.3V OD/PP		I/O
SDIO_LED	SDIO LED. Used to drive an external LED to indicate when transfers occur on the bus.	CMOS 3.3V	max 1 mA	O
SDIO_WP	SDIO Write Protect. This signal denotes the state of the write-protect tab on SD cards.	CMOS 3.3V		I/O
SDIO_PWR#	SDIO Power Enable. This signal is used to enable the power being supplied to a SD/MMC card device.	CMOS 3.3V		O
SDIO_DAT0-7	SDIO Data lines. These signals operate in push-pull mode.	CMOS 3.3V PP		I/O

3.1.7 High Definition Audio Signals/AC'97

Table 3-9 Signal Definition HDA/AC'97

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
HDA_RST# I2S_RST#	HD Audio/AC'97 Codec Reset. Multiplexed with I2S Codec Reset.	CMOS 3.3V		O
HDA_SYNC I2S_WS	Serial Bus Synchronization. Multiplexed with I2S Word Select from Codec.	CMOS 3.3V		O
HDA_BCLK I2S_CLK	HD Audio/AC'97 24 MHz Serial Bit Clock from Codec. Multiplexed with I2S Serial Data Clock from Codec.	CMOS 3.3V		O
HDA_SDO I2S_SDO	HD Audio/AC'97 Serial Data Output to Codec. Multiplexed with I2S Serial Data Output from Codec.	CMOS 3.3V		O
HDA_SDI I2S_SDI	HD Audio/AC'97 Serial Data Input from Codec. Multiplexed with I2S Serial Data Input from Codec.	CMOS 3.3V		I

Note

The High Definition Audio or AC'97 or I2S interface are features that are platform dependent and therefore may not be available in all cases.

3.1.8 LVDS Flat Panel Signals

Table 3-10 Signal LVDS

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
LVDS_PPEN	Controls panel power enable.	CMOS 3.3V	max 1 mA	O
LVDS_BLEN	Controls panel backlight enable.	CMOS 3.3V	max 1 mA	O
LVDS_BLT_CTRL /GP_PWM_OUT0	Primary functionality is to control the panel backlight brightness via pulse width modulation (PWM). When not in use for this primary purpose it can be used as General Purpose PWM Output.	CMOS 3.3V		O
LVDS_A0+ LVDS_A0-	LVDS primary channel differential pair 0.	LVDS		O
eDP0_TX0+ eDP0_TX0-	Display Port primary channel differential pair 0.	LVDS		O
LVDS_A1+ LVDS_A1-	LVDS primary channel differential pair 1.	LVDS		O
eDP0_TX1+ eDP0_TX1-	Display Port primary channel differential pair 1.	LVDS		O
LVDS_A2+ LVDS_A2-	LVDS primary channel differential pair 2.	LVDS		O
eDP0_TX2+ eDP0_TX2-	Display Port primary channel differential pair 2.	LVDS		O
LVDS_A3+ LVDS_A3-	LVDS primary channel differential pair 3.	LVDS		O
eDP0_TX3+ eDP0_TX3-	Display Port primary channel differential pair 3.	LVDS		O
LVDS_A_CLK+ LVDS_A_CLK-	LVDS primary channel differential pair clock lines.	LVDS		O
eDP0_AUX+ eDP0_AUX-	Display Port primary auxiliary channel.	LVDS		O
LVDS_B0+ LVDS_B0-	LVDS secondary channel differential pair 0.	LVDS		O
eDP1_TX0+ eDP1_TX0-	Display Port secondary channel differential pair 0.	LVDS		O
LVDS_B1+ LVDS_B1-	LVDS secondary channel differential pair 1.	LVDS		O
eDP1_TX1+ eDP1_TX1-	Display Port secondary channel differential pair 1.	LVDS		O
LVDS_B2+ LVDS_B2-	LVDS secondary channel differential pair 2.	LVDS		O
eDP1_TX2+ eDP1_TX2-	Display Port secondary channel differential pair 2.	LVDS		O
LVDS_B3+ LVDS_B3-	LVDS secondary channel differential pair 3.	LVDS		O
eDP1_TX3+ eDP1_TX3-	Display Port secondary channel differential pair 3.	LVDS		O
LVDS_B_CLK+ LVDS_B_CLK-	LVDS secondary channel differential pair clock lines.	LVDS		O

eDP1_AUX+ eDP1_AUX-	Display Port secondary auxiliary channel.	LVDS		O
LVDS_DID_CLK GP2_I2C_CLK	Primary functionality is DisplayID DDC clock line used for LVDS flat panel detection. If the primary functionality is not used, it can be used as a General Purpose I²C bus clock line.	CMOS 3.3V OD		I/O
LVDS_DID_DAT GP2_I2C_DAT	Primary functionality DisplayID DDC data line used for LVDS flat panel detection. If the primary functionality is not used, it can be used as a General Purpose I²C bus data line.	CMOS 3.3V OD		I/O
LVDS_BLC_CLK eDP1_HPD#	Control clock signal for external SSC clock chip. If the primary functionality is not used, it can be used as an emedded DisplayPort secondary Hotplug detection.	CMOS 3.3V OD		I/O
LVDS_BLC_DAT eDP0_HPD#	Control data signal for external SSC clock chip. If the primary functionality is not used, it can be used as an emedded DisplayPort primary Hotplug detection.	CMOS 3.3V OD		I/O

The LVDS flat panel configuration within the BIOS of the Qseven® module shall be implemented in accordance to the DisplayID specification that is under development within the Video Electronics Standards Association (VESA). For more information about the LVDS flat panel configuration with DisplayID refer to the specification 'Display Identification Data (DisplayID) Structure Version 1.0' that is available on the webpage of the Video Electronics Standards Association (VESA).

Note

The LVDS interface can be used either as a single channel or as a dual channel, depending on the properties of the platform used for the Qseven® / µQseven module.

It is also possible to use the LVDS interface as two independent single LVDS channels. To do this, it is recommended to set the configuration of the LVDS display with an external EEPROM.

3.1.9 DisplayPort Interface Signals

DisplayPort is an open, industry standard digital display interface, that is under development within the Video Electronics Standards Association (VESA). The DisplayPort specification defines a scalable digital display interface with optional audio and content protection capability. It defines a license-free, royalty-free, state-of-the-art digital audio/video interconnect, intended to be used primarily between a computer and its display monitor.

Table 3-11 Signal Definition DisplayPort

Signal	Shared With	Description	I/O Type	I_{OL}/I_{IL}	I/O
DP_LANE3- DP_LANE3+	TMDS_CLK- TMDS_CLK+	DisplayPort differential pair lines lane 3.	PCIE		O
DP_LANE2- DP_LANE2+	TMDS_LANE0- TMDS_LANE0+	DisplayPort differential pair lines lane 2.	PCIE		O
DP_LANE1- DP_LANE1+	TMDS_LANE1- TMDS_LANE1+	DisplayPort differential pair lines lane 1.	PCIE		O
DP_LANE0- DP_LANE0+	TMDS_LANE2- TMDS_LANE2+	DisplayPort differential pair lines lane 0.	PCIE		O
DP_AUX- DP_AUX+		Auxiliary channel used for link management and device control. Differential pair lines.	PCIE		I/O
DPHDMI_HPD#		Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

Note

Support of the DisplayPort interface is chipset dependent and therefore may not be available on all Qseven® modules. The DisplayPort interface signals are shared with the signals for the TMDS interface.

3.1.10 HDMI Interface Signals

High-Definition Multimedia Interface (HDMI) is a licensable compact audio/video connector interface for transmitting uncompressed digital streams. HDMI encodes the video data into TMDS for digital transmission and is backward-compatible with the single-link Digital Visual Interface (DVI) carrying digital video. Both HDMI and DVI were pioneered by Silicon Image and are based on TMDS®, Silicon Image's powerful, high-speed, serial link technology.

Table 3-12 Signal Definition HDMI

Signal	Shared With	Description	I/O Type	I_{OL}/I_{IL}	I/O
TMDS_CLK- TMDS_CLK+	DP_LANE3- DP_LANE3+	TMDS differential pair clock lines.	TMDS		O
TMDS_LANE0- TMDS_LANE0+	DP_LANE2- DP_LANE2+	TMDS differential pair lines lane 0.	TMDS		O
TMDS_LANE1- TMDS_LANE1+	DP_LANE1- DP_LANE1+	TMDS differential pair lines lane 1.	TMDS		O
TMDS_LANE2- TMDS_LANE2+	DP_LANE0- DP_LANE0+	TMDS differential pair lines lane 2.	TMDS		O
HDMI_CTRL_CLK		DDC based control signal (clock) for HDMI device. ***Note:*** *Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.*	CMOS 3.3V OD		I/O
HDMI_CTRL_DAT		DDC based control signal (data) for HDMI device. ***Note:*** *Level shifters must be implemented on the carrier board for this signal in order to be compliant with the HDMI Specification.*	CMOS 3.3V OD		I/O
DP_HDMI_HPD#		Hot plug detection signal that serves as an interrupt request.	CMOS 3.3V		I

Note

Support of the TMDS interface is chipset dependent and therefore may not be available on all Qseven® modules. The TMDS interface signals are shared with the signals for the DisplayPort interface.

3.1.11 LPC Interface Signals

The Low Pin Count (LPC) bus interface is a cost-efficient, low-speed interface designed to support low-speed legacy devices such as a Super I/O controller or a firmware hub device.

Table 3-13 Signal Definition LPC

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
LPC_AD[0..3] GPIO[0..3]	Multiplexed Command, Address and Data. General purpose input/output [0..3]	CMOS 3.3V		I/O
LPC_FRAME# GPIO5	LPC frame indicates the start of a new cycle or the termination of a broken cycle. General purpose input/output 5.	CMOS 3.3V		I/O
LPC_LDRQ# GPIO7	LPC DMA request. General purpose input/output 7.	CMOS 3.3V		I/O
LPC_CLK GPIO4	LPC clock. General purpose input/output 4.	CMOS 3.3V		I/O
SERIRQ GPIO6	Serialized Interrupt. General purpose input/output 6.	CMOS 3.3V		I/O

3.1.12 SPI Interface Signals

The Serial Peripheral Interface (SPI) is a 4-pin interface that provides a potentially lower-cost alternative for system devices such as EEPROM and flash components.

Table 3-14 Signal Definition SPI

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
SPI_MOSI	Master serial output/Slave serial input signal. SPI serial output data from Qseven® module to the SPI device.	CMOS 3.3V		O
SPI_MISO	Master serial input/Slave serial output signal. SPI serial input data from the SPI device to Qseven® module.	CMOS 3.3V		I
SPI_SCK	SPI clock output.	CMOS 3.3V		O
SPI_CS0#	SPI chip select 0 output.	CMOS 3.3V		O
SPI_CS1#	SPI Chip Select 1 signal is used as the second chip select when two devices are used. Do not use when only one SPI device is used.	CMOS 3.3V		O

3.1.13 CAN Bus Interface Signals

Controller Area Network (CAN or CAN-bus) is a message based protocol designed specifically for automotive applications but now is also used in other areas such as industrial automation and medical equipment.

Table 3-15 Signal Definition CAN Bus

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
CAN0_TX	CAN (Controller Area Network) TX output for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	CMOS 3.3V		O
CAN0_RX	RX input for CAN Bus channel 0. In order to connect a CAN controller device to the Qseven® module's CAN bus it is necessary to add transceiver hardware to the carrier board.	CMOS 3.3V		I

Note

If the CAN Bus interface is not used, and/or the Qseven® module's chipset does not support CAN Bus, then these pins shall be left unconnected.

3.1.14 Input Power Pins

Table 3-16 Signal Definition Input Power

Signal	Description	I/O
VCC	Power Supply +5VDC ±5%.	P
VCC_5V_SB	Standby Power Supply +5VDC ±5%.	P
VCC_RTC	3 V backup cell input. VCC_RTC should be connected to a 3V backup cell for RTC operation and storage register non-volatility in the absence of system power. (VCC_RTC = 2.4 - 3.3 V).	P
GND	Power Ground.	P

3.1.15 Power Control Signals

Table 3-17 Signal Definition Power Control

Signal	Description of Power Control signals	I/O Type	I_{OL}/I_{IL}	I/O
PWGIN	High active input for the Qseven® module indicates that all power rails located on the carrier board are ready for use.	CMOS 5V	≥ 4 mA	I
PWRBTN#	Power Button: Low active power button input. This signal is triggered on the falling edge.	CMOS 3.3V Standby	≥ 10 mA	I

3.1.16 Power Management Signals

Table 3-18 Signal Definition Power Management

Signal	Description of Power Management signals	I/O Type	I_{OL}/I_{IL}	I/O
RSTBTN#	Reset button input. This input may be driven active low by an external circuitry to reset the Qseven® module.	CMOS 3.3V	≥ 10 mA	I
BATLOW#	Battery low input. This signal may be driven active low by external circuitry to signal that the system battery is low or may be used to signal some other external battery management event.	CMOS 3.3V Suspend	≥ 10 mA	I
WAKE#	External system wake event. This may be driven active low by external circuitry to signal an external wake-up event.	CMOS 3.3V Suspend	≥ 10 mA	I
SUS_STAT#	Suspend Status: indicates that the system will be entering a low power state soon.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S3#	S3 State: This signal shuts off power to all runtime system components that are not maintained during S3 (Suspend to Ram), S4 or S5 states. The signal SUS_S3# is necessary in order to support the optional S3 cold power state.	CMOS 3.3V Suspend	max. 1 mA	O
SUS_S5#	S5 State: This signal indicates S4 or S5 (Soft Off) state.	CMOS 3.3V Suspend	max. 1 mA	O
SLP_BTN#	Sleep button. Low active signal used by the ACPI operating system to transition the system into sleep state or to wake it up again. This signal is triggered on falling edge.	CMOS 3.3V Suspend	≥ 10 mA	I
LID_BTN#	LID button. Low active signal used by the ACPI operating system to detect a LID switch and to bring system into sleep state or to wake it up again. Open/Close state may be software configurable.	CMOS 3.3V Suspend	≥ 10 mA	I

Note

It must be guaranteed that all the carrier board power rails, that are generated out of the VCC power rail, will be enabled by the SUS_S3# signal.

3.1.17 Miscellaneous Signals

Table 3-19 Signal Definition Miscellaneous

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
WDTRIG#	Watchdog trigger signal. This signal restarts the watchdog timer of the Qseven® module on the falling edge of a low active pulse.	CMOS 3.3V	≥ 10 mA	I
WDOUT	Watchdog event indicator. High active output used for signaling a missing watchdog trigger. Will be deasserted by software, system reset or a system power down.	CMOS 3.3V	max. 5 mA	O
GP0_I2C_CLK	General Purpose I²C bus #0 clock line.	CMOS 3.3V OD		I/O
GP0_I2C_DAT	General Purpose I²C bus #0 data line.	CMOS 3.3V OD		I/O
SMB_CLK GP1_I2C_CLK	Clock line of System Management Bus. Multiplexed with General Purpose I²C bus #1 clock line.	CMOS 3.3V OD Suspend		I/O
SMB_DAT GP1_I2C_DAT	Data line of System Management Bus. Multiplexed with General Purpose I²C bus #1 data line.	CMOS 3.3V OD Suspend		I/O
SMB_ALERT#	System Management Bus Alert input. This signal may be driven low by SMB devices to signal an event on the SM Bus.	CMOS 3.3V OD Suspend		I/O
SPKR GP_PWM_OUT2	Primary functionality is output for audio enunciator, the “speaker” in PC AT systems. When not in use for this primary purpose it can be used as General Purpose PWM Output.	CMOS 3.3V		O
BIOS_DISABLE# /BOOT_ALT#	Module BIOS disable input signal. Pull low to disable module's on-board BIOS. Allows off-module BIOS implementations. This signal can also be used to disable standard boot firmware flash device and enable an alternative boot firmware source, for example a boot loader.	CMOS 3.3V		I
RSVD	Do not connect.			NC
GP_1-Wire_Bus	General Purpose 1-Wire bus interface. Can be used for consumer electronics control bus (CEC) of HDMI	CMOS 3.3V		I/O

3.1.18 Manufacturing Signals

Table 3-20 Signal Definition Manufacturing

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
MFG_NC0	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TCK signal for boundary scan purposes during production or as a vendor specific control signal. When used as a vendor specific control signal the multiplexer must be controlled by the MFG_NC4 signal.	n.a.	n.a.	n.a.
MFG_NC1	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDO signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_TX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	n.a.	n.a.	n.a.
MFG_NC2	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TDI signal for boundary scan purposes during production. May also be used, via a multiplexer, as a UART_RX signal to connect a simple UART for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	n.a.	n.a.	n.a.
MFG_NC3	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TMS signal for boundary scan purposes during production. May also be used, via a multiplexer, as vendor specific BOOT signal for firmware and boot loader implementations. In this case the multiplexer must be controlled by the MFG_NC4 signal.	n.a.	n.a.	n.a.
MFG_NC4	This pin is reserved for manufacturing and debugging purposes. May be used as JTAG_TRST# signal for boundary scan purposes during production. May also be used as control signal for a multiplexer circuit on the module enabling secondary function for MFG_NC0..3 (JTAG / UART). When MFG_NC4 is high active it is being used for JTAG purposes. When MFG_NC4 is low active it is being used for UART purposes.	n.a.	n.a.	n.a.

Note

The MFG_NC0..4 pins are reserved for manufacturing and debugging purposes. It's recommended to route the signals to a connector on the carrier board.

The carrier board must not drive the MFG_NC-pins or have pull-up or pull-down resistors implemented for these signals. MFG_NC0...4 are defined to have a voltage level of 3.3V. It must be ensured that the carrier board has the correct voltage levels for JTAG/UART signals originating from the module. For this reason, a level shifting device may be required on the carrier board to guarantee that these voltage levels are correct in order to prevent damage to the module.

More information about implementing a carrier board multiplexer can be found in the Qseven® Design Guide.

For more information about vendor specific functionality of MFG_NC0...4, refer to the vendor's module documentation.

3.1.19 Thermal Management Signals

Table 3-21 Signal Definition Thermal Management

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
THRM#	Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling.	CMOS 3.3V		I
THRMTRIP#	Thermal Trip indicates an overheating condition of the processor. If *'THRMTRIP#'* goes active the system immediately transitions to the S5 State (Soft Off).	CMOS 3.3V		O

3.1.20 Fan Control Implementation

Table 3-22 Signal Definition Fan Control

Signal	Description	I/O Type	I_{OL}/I_{IL}	I/O
FAN_PWMOUT /GP_PWM_OUT1	Primary functionality is fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the Fan's RPM based on the CPU's die temperature. When not in use for this primary purpose it can be used as General Purpose PWM Output.	CMOS 3.3V OC		O
FAN_TACHOIN /GP_TIMER_IN	Primary functionality is fan tachometer input. When not in use for this primary purpose it can be used as General Purpose Timer Input.	CMOS 3.3V		I

3.2 Input Power Requirements

Qseven® modules are designed to be driven with a single +5V input power rail. Additionally, two optional power rails are specified by Qseven® to provide a +5V standby voltage on the Qseven® module as well as a +3V Real Time Clock (RTC) supply voltage, which is provided by a battery cell located on the carrier board.

If the carrier board does not require standby functionality, then the +5V standby power rail can be omitted. The same applies to the +3V RTC battery voltage. If no RTC/CMOS backup functionality is required by the system, then the +3V RTC supply battery voltage can be omitted.

Table 3-23 Input Power Characteristics

Power Rail	Nominal Input	Input Range	Max Input Ripple
VCC	+5V	+4.75V - +5.25V	±50 mV
VCC_5V_SB	+5V	+4.75V - +5.25V	±50 mV
VCC_RTC	+3V	+2.0V - +3.3V	±20 mV

Note

If the standby 5V power rail 'VCC_5V_SB' is not provided by the carrier board, then the VCC_5V_SB pins (pins 205-206) of the Qseven® module must be connected with the main VCC power rail pins (pins 211-230).

3.2.1 Input Power Sequencing

Qseven® input power sequencing requirements are as follows:

Start Sequence:

- VCC_RTC must come up at the same time or before VCC_5V_SB comes up.
- VCC_5V_SB must come up at the same time or before VCC comes up.
- PWGIN must be active at the same time or after VCC comes up.

Stop Sequence:

- PWGIN must be inactive at the same time or before VCC goes down
- VCC must go down at the same time or before VCC_5V_SB goes down
- VCC_5V_SB must go down at the same time or before VCC_RTC goes down

Figure 3-1 Input Power Sequencing

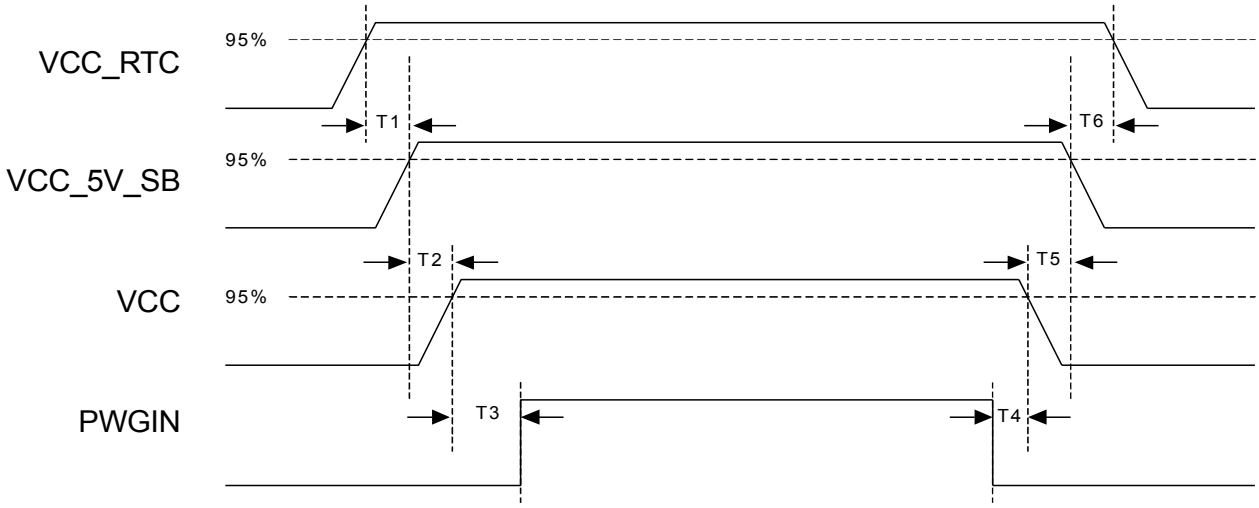


Table 3-24: Input Power Sequencing

Item	Description	Value
T1	VCC_RTC rise to VCC_5V_SB rise	≥ 0 ms
T2	VCC_5V_SB rise to VCC rise	≥ 0 ms
T3	VCC rise to PWGIN rise	≥ 0 ms
T4	PWGIN fall to VCC fall	≥ 0 ms
T5	VCC fall to VCC_5V_SB fall	≥ 0 ms
T6	VCC_5V_SB fall to VCC_RTC fall	≥ 0 ms

4 Qseven® Signaling Budgets

4.1 PCI Express

According to the PCI Express Base Specification Revision 1.1, a total available interconnect loss budget of 13.2 dB is allowed between the PCI Express host device on the Qseven® CPU module and the PCI Express device on the carrier board, ExpressCard or PCI Express add-in card.

The electrical characteristic of the Qseven® module is defined in terms of electrical insertion loss budgets. This budget allocation decouples the electrical specification for the carrier board designer and the Qseven® module vendor. Unless otherwise noted, the specifications contained herein apply to all high-speed signals of each interface width definition. The signaling rate for encoded data is 2.5 Gigabit transfers/s and the signaling is point-to-point.

4.1.1 Qseven® Module PCI Express Budget Allocation

Figure 4-1 PCI Express Budget Allocation

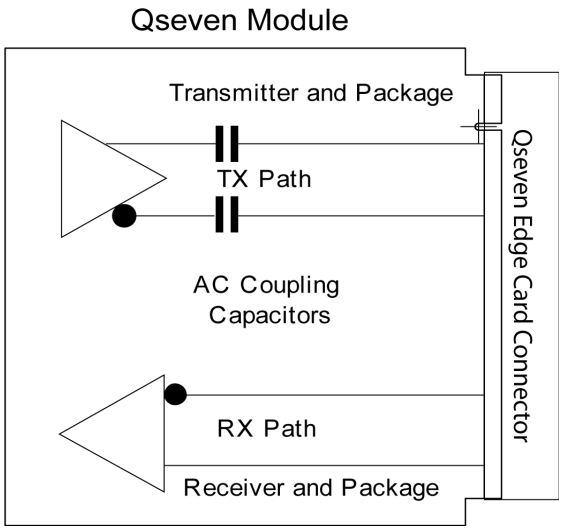


Table 4-1 PCI Express Budget Allocation

Segment	Loss Budget Value at 1.25 GHz	max. Trace Length	Comments
Qseven® Module (TX path)	< 2.5 dB	2 inches	Note 1, 2, 3, 4, 5, 6
Qseven® Module (RX path)	< 2.1 dB	2 inches	Note 1, 2, 4, 5, 6

Notes

1. *The PCI Express Base Specification allows an interconnect loss of 13.2 dB for 1.25 GHz signals. The allocated Qseven® loss budget does not include crosstalk and impedance mismatch. As a guide for design and simulation, the PCI Express CEM Specification recommends to subtract 5.2 dB from the 13.2 dB budget, to cover crosstalk and impedance mismatch for the total interconnect path. The 5.2dB budget also includes the overall 1.25dB guard band as recommended by the PCI CEM Specification.*

2. *This budget also includes the connector on the carrier board. The budget allocated to the Qseven® connector is 1.0dB @ 1.25GHz.*

3. *The TX path budget includes the additional damping of the DC decoupling capacitors.*

4. *Typical damping of the PCB trace of 0.35dB/inch @ 1.25GHz (common value for FR-4 based material).*

5. *Maximum 2 vias per trace for a RX path and maximum 4 vias per trace for a TX path on the connection from the core logic chipset to the Qseven® connector on the Qseven® module.*

6. *Trace routing is implemented according to the design rules for high speed differential traces.*

4.1.2 PCI Express Insertion Loss Budget

Figure 4-2PCI Express Link Topology 1

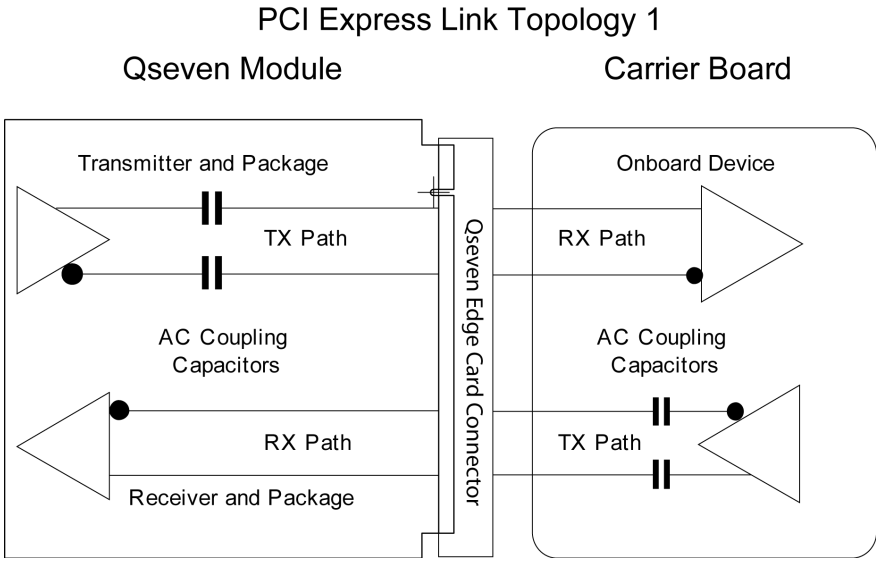
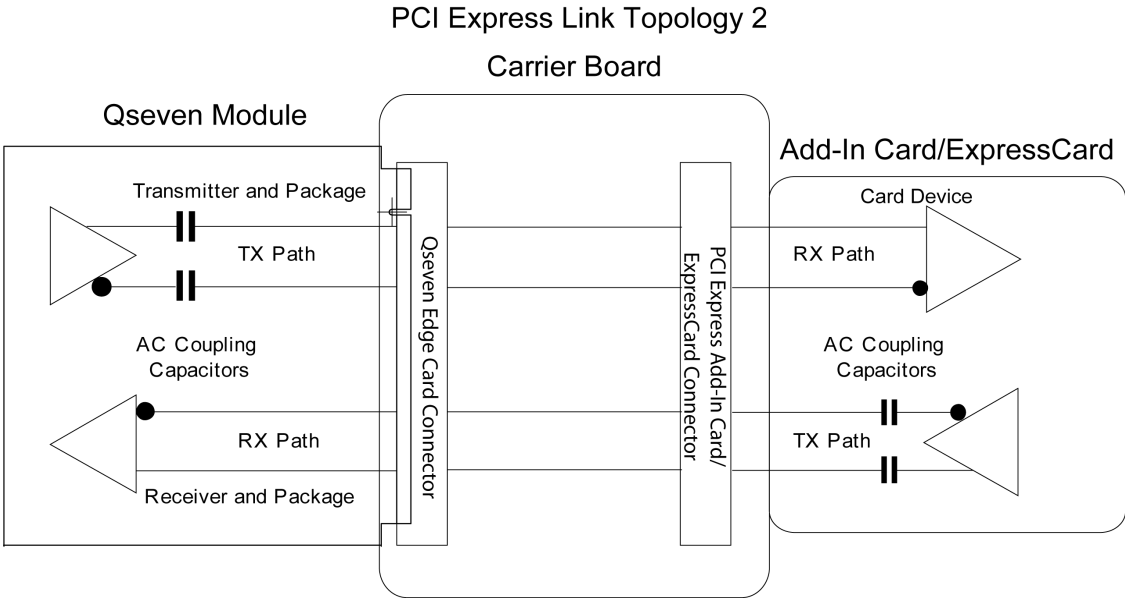


Figure 4-3 PCI Express Link Topology 2



Note

The term "TX-path" that is used in Table 4-2 refers to the signal path from the PCI Express transmitter on the Qseven® module to the PCI Express receiver, of an onboard device or on an add-in card, on the Qseven® carrier board.

The term "RX-path" that is used in Table 4-2 refers to the signal path from the PCI Express transmitter, of an onboard device or on an add-in card on the Qseven® carrier board, to the PCI Express receiver on the Qseven® module.

Table 4-2 Carrier Board PCI Express Insertion Loss Budget

Segment	Loss Budget Value at 1.25 GHz (dB)	Max. Trace Length	Comments
Carrier Board Topology 1 (TX path)	5.5dB	14.5 inches	Carrier Board with onboard PCI Express device
Carrier Board Topology 1 (RX path)	5.9dB	15.7 inches	Carrier Board with onboard PCI Express device
Carrier Board Topology 2 (TX path)	4.1dB	7.7 inches	Carrier Board with PCI Express Connector for Add-In Card or ExpressCard
Carrier Board Topology 2 (RX path)	4.1dB	7.7 inches	Carrier Board with PCI Express Connector for Add-In Card or ExpressCard

The trace lengths presented in Table 4-2 are based on the following assumptions:

- Typical damping of the PCB trace of 0.35dB/inch @ 1,25GHz (common value for FR-4 based material)
- The RX path budget includes the additional damping of the DC decoupling capacitors and 2 additional vias for connecting the decoupling capacitors
- Maximum 2 vias per trace for a RX path and maximum 4 vias per trace for a TX path on the connection from the the Qseven®connector on the Qseven®carrier board to an onboard device
- Maximum 2 vias per trace for a RX path and maximum 2 vias per trace for a TX path on the connection from the Qseven®connector on the Qseven®carrier board to a PCI Express extension socket that is compliant to the properties defined in the PCI Express Card Electromechanical Specification (this includes standard PCI Express cards as well as ExpressCards).
- Trace routing is implemented according to the design rules for high speed differential traces.

The values in Table 4-2 are derived from a signal integrity simulation and reflect a worst case scenario. The values given are design rules for a maximum interoperability between Qseven®modules from different vendors and customer specific Qseven® carrier boards and shall be observed. Designers that face the necessity to deviate from the given values have to conduct a suitable signal integrity simulation to guarantee compliance to the Qseven®specification and the underlying PCI Express specification. Carrier boards that do not follow the design rules presented in this specification and those that have not been simulated are not considered Qseven®compliant.

For carrier board designers that want to set up a simulation environment they should contact their Qseven®module vendor to obtain an Qseven®module model for signal integrity simulation.

Note

For USB3.0, HDMI and DisplayPort interface signals the description offered in this section is also applicable. Design guidelines for high speed differential traces can be found in the Qseven® Design Guide.

4.2 Serial ATA

4.2.1 Serial ATA Insertion Loss Budget

As outlined in the Serial ATA Specification, the following insertion loss budgets for the SATA implementation on the Qseven® module and carrier board shall be observed. Figure 4-4 shows a typical Serial ATA link topology of a Qseven® based application.

Figure 4-4 Serial ATA Link Topology

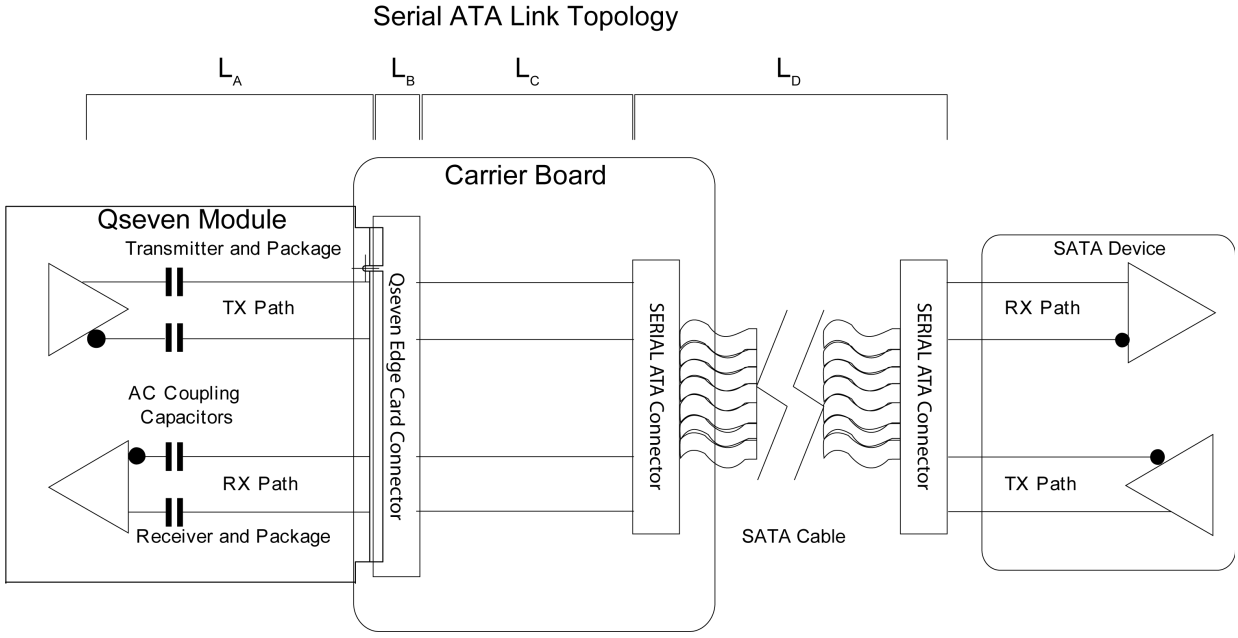


Table 4-3 SATA Gen 1 Loss Budget Allocation

Segment	Loss Budget Value at 0.75 GHz (dB)	Max. Trace Length	Comments
L_A	0.5 dB	2.5 inches	Module Trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40 dB		
L_B	0.40 dB		MXM Connector @ 0.75 GHz
L_C	1.55 dB	7.2	Carrier Board Trace @ 0.28 dB / GHz / inch
Total	2.85 dB		

Note

SATA specification 3.1 defines the signal budget from chip to mated connector.

The trace lengths presented in Table 4-3 are based on the following assumptions:

- Typical damping of the PCB trace of 0.42dB/inch @ 1,5GHz (common value for FR-4 based material)
- The budget includes the additional damping of the DC decoupling and the Qseven®

connector losses.

- Trace routing is implemented according to the design rules for high speed differential traces.

Table 4-4 SATA Gen2 Loss Budget Allocation

Segment	Loss Budget Value at 1.5 GHz (dB)	Max. Trace Length	Comments
L_A	1.05 dB	2.5 inches	Module Trace @ 0.28 dB / GHz / inch
Coupling Caps	0.40 dB		
L_B	0.50 dB		MXM Connector @ 1.5 GHz
L_C	1,05 dB	2.5 inches	Carrier Board Trace @ 0.28 dB / GHz / inch
Total	3.00 dB		

Note

SATA specification 3.1 defines the signal budget from chip to mated connector.

4.3 USB 2.0

4.3.1 USB 2.0 Insertion Loss Budget

Figure 4-5 USB 2.0 Link Topology

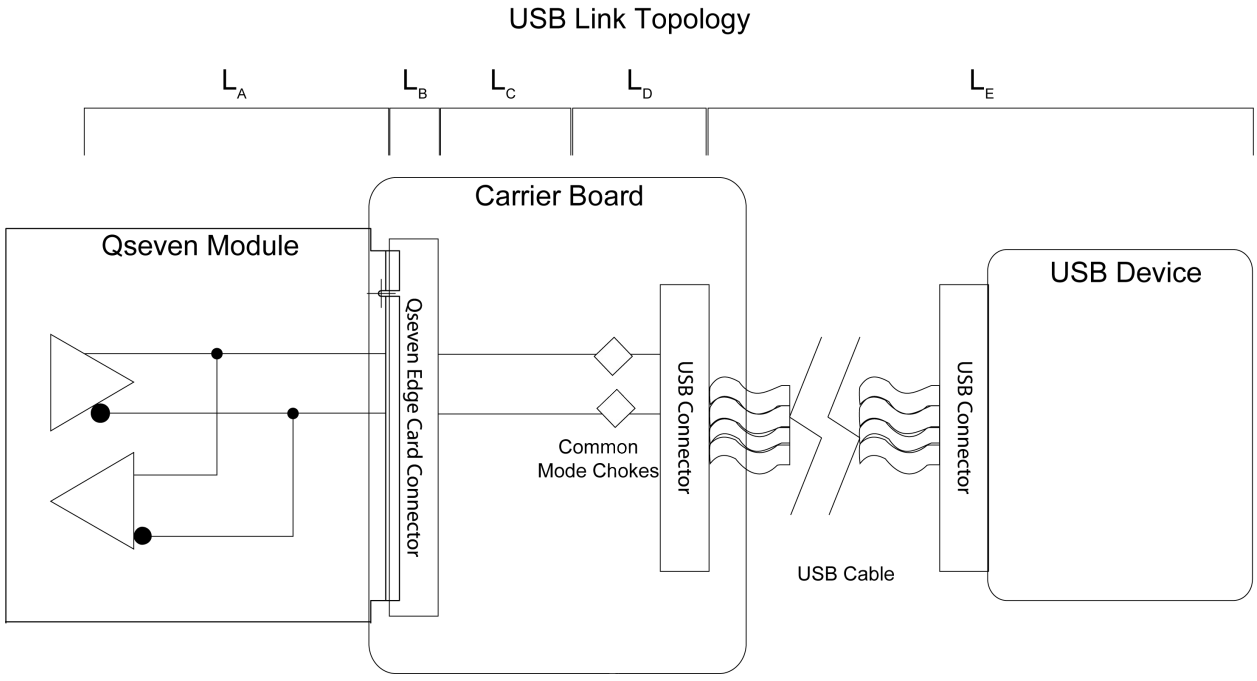


Table 4-5 USB 2.0 Loss Budget Allocation

Segment	Loss Budget Value at 240 MHz	max. Trace Length	Comments
L_A	0.4 dB	6 inches	Module Trace @ 0.28 dB / GHz / inch
L_B	0.05 dB		MXM Connector at 240 MHz
L_C	1 dB	14 inches	Carrier Board Trace @ 0.28 dB / GHz / inch
L_D	1.00 dB		USB Connector and Ferrite Loss
L_E	3,6 dB		USB cable and far end connector loss, per source specification.
Total	6.05 dB		

Qseven® USB implementations should conform to insertion loss values less than or equal to those shown in Table 4-5 above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the USB specification.

"Device Down" implementations, in which the USB target device is implemented on the carrier board, may add the ferrite and USB connector insertion loss values to the carrier board budget.

The carrier board insertion loss budget then becomes LC + LD, or 2.68 dB.

4.4 Gigabit Ethernet

4.4.1 Gigabit Ethernet Insertion Loss Budget

Figure 4-6 Gigabit Ethernet Link Topology

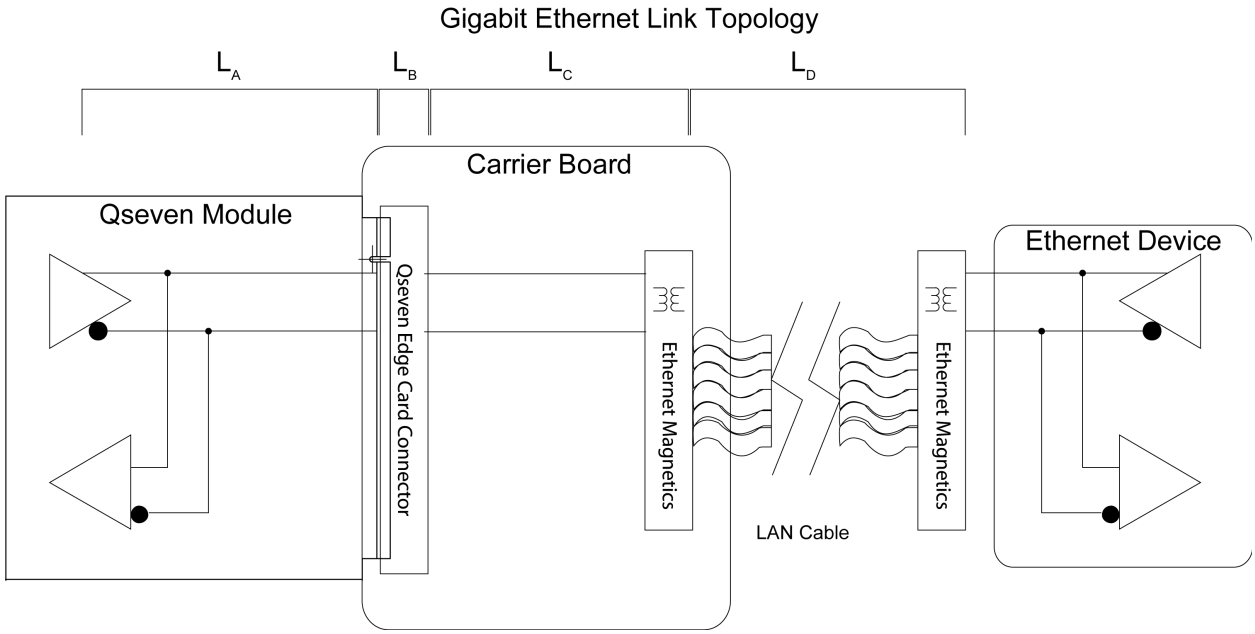


Table 4-6 Gigabit Ethernet Loss Budget Allocation

Segment	Loss Budget Value at 100 MHz	max. Trace Length	Comments
L_A	0.08 dB	2 inches	Module trace @ 0.28 dB / GHz / inch
L_B	0.02 dB		MXM connector at 100 MHz
L_C	0.15 dB	4 inches	Carrier Board trace @ 0.28 dB / GHz / inch
L_D	24.00 dB		Cable and cable connectors, integrated magnetics, per source spec
Total	24.25 dB		

Qseven® Ethernet implementations should conform to insertion loss values less than or equal to those shown in Table 4-6 above. The insertion loss values shown account for frequency dependent material losses only. Cross talk losses are separate from material losses in the Gigabit Ethernet specification.

“Device Down” implementations, in which the Ethernet target device is implemented on the carrier board (for instance, an Ethernet switch), may add the insertion loss for the RJ45 Ethernet jack and integrated magnetics to the carrier board budget. This insertion loss value is typically 1 dB. The carrier board insertion loss budget then becomes LC + 1 dB, or 1.15 dB.

5 Software Definitions

5.1 BIOS Implementations

5.1.1 LPC Super I/O Support

The Qseven® BIOS firmware shall include integrated support for the following external LPC Super I/O controllers in order to provide additional legacy COM ports.

Support for the COM ports of the following Super I/Os shall be implemented in the Qseven® module BIOS:

1. Winbond W83627DHG LPC Super I/O with 2 COM ports
2. SMSC SCH3114 LPC Super I/O with 4 COM ports

If any of the additional functionality of the Super I/O is required by the application, then it may be implemented via the application's software program. There are Super I/O functions that can be configured by hardware straps, which is defined within the datasheet of that particular Super I/O (for example PS/2 keyboard functionality). By default, these functions must be disabled if the Super I/O is to be implemented on a Qseven® module.

The base address for these Super I/O controllers shall be 0x2E to be sure that the legacy COM port devices of the Super I/O controller can be initialized by the BIOS.

5.2 Embedded Application Programming Interface

5.2.1 General Information

Qseven® embedded computer modules are equipped with additional functions for industrial applications. These functions are provided through the use of an API (Application Program Interface) called Embedded Application Programming Interface (EAPI) that is offered and supported by the PICMG®. The EAPI definition is open to be used for different embedded form factors including Qseven®.

This API is provided via a shared library. Examples of this include I²C Bus, LCD brightness control, BIOS user storage area and the reading of system temperatures.

The Embedded Application Programming Interface offered by the PICMG® can be found at the PICMG® website via the following links:

http://www.picmg.org/v2internal/resourcepage2.cfm?id=3
http://www.picmg.org/pdf/COM_EAPI_R1_0.pdf

6 Industry Specifications

The list below provides links to industry specifications used to define the Qseven® interface specification.

Table 6-1 Industry Specifications

Specification	Description	Link
1000BASE T	IEEE standard 802.3ab 1000BASE T Ethernet	www.ieee.org/portal/site
ACPI	Advanced Configuration and Power Interface Specification Rev. 3.0a	www.acpi.info
DisplayID	Display Identification Data (DisplayID) Structure, Version 1.0	www.vesa.org
DisplayPort	DisplayPort Standard - Version 1.1a	www.vesa.org
DVI	Digital Visual Interface, Rev 1.0, April 2, 1999, Digital Display Working Group	www.ddwg.org
HDA	High Definition Audio Specification, Rev. 1.0	www.intel.com/standards/hdaudio
I2C	The I2C Bus Specification, Version 2.1, January 2000, Philips Semiconductors, Document order number 9398 393 4001 1	www.semiconductors.philips.com
I2S	The I2S Bus Specification Version	www.semiconductors.philips.com
IEEE 802.3-2002	IEEE Standard for Information technology, Telecommunications and information exchange between systems—Local and metropolitan area networks—Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications	www.ieee.org
LPC	Low Pin Count Interface Specification, Revision 1.1 (LPC)	developer.intel.com/design/chipsets/industry/lpc.htm
LVDS	Open LVDS Display Interface (Open LDI) Specification, v0.95, May 13, 1999, Copyright © National Semiconductor	www.national.com
LVDS	LVDS Owner's Manual	www.national.com
LVDS	ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001.	www.ansi.org
PCI Express	PCI Express Base Specification, Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved	www.pcisig.com
PCI Express	PCI Express Base Specification, Revision 1.1 PCI Express Card Electromechanical Specification, Revision 1.1	www.pcisig.com/specifications
SATA	Serial ATA: High Speed Serialized AT Attachment, Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc., Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved	www.sata-io.org
SATA	Serial ATA Specification, Revision 1.0a	www.serialata.org
Smart Battery	Smart Battery Data Specification, Revision 1.1, December 11, 1998	www.sbs-forum.org

SMBUS	System Management Bus (SMBUS) Specification, Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, PowerSmart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved	www.smbus.org
USB	Universal Serial Bus (USB) Specification, Revision 2.0	www.usb.org/home

